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Crappie_IAH MB Schematics Document

Alder Lake H45 with DDR4

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2022-12-05

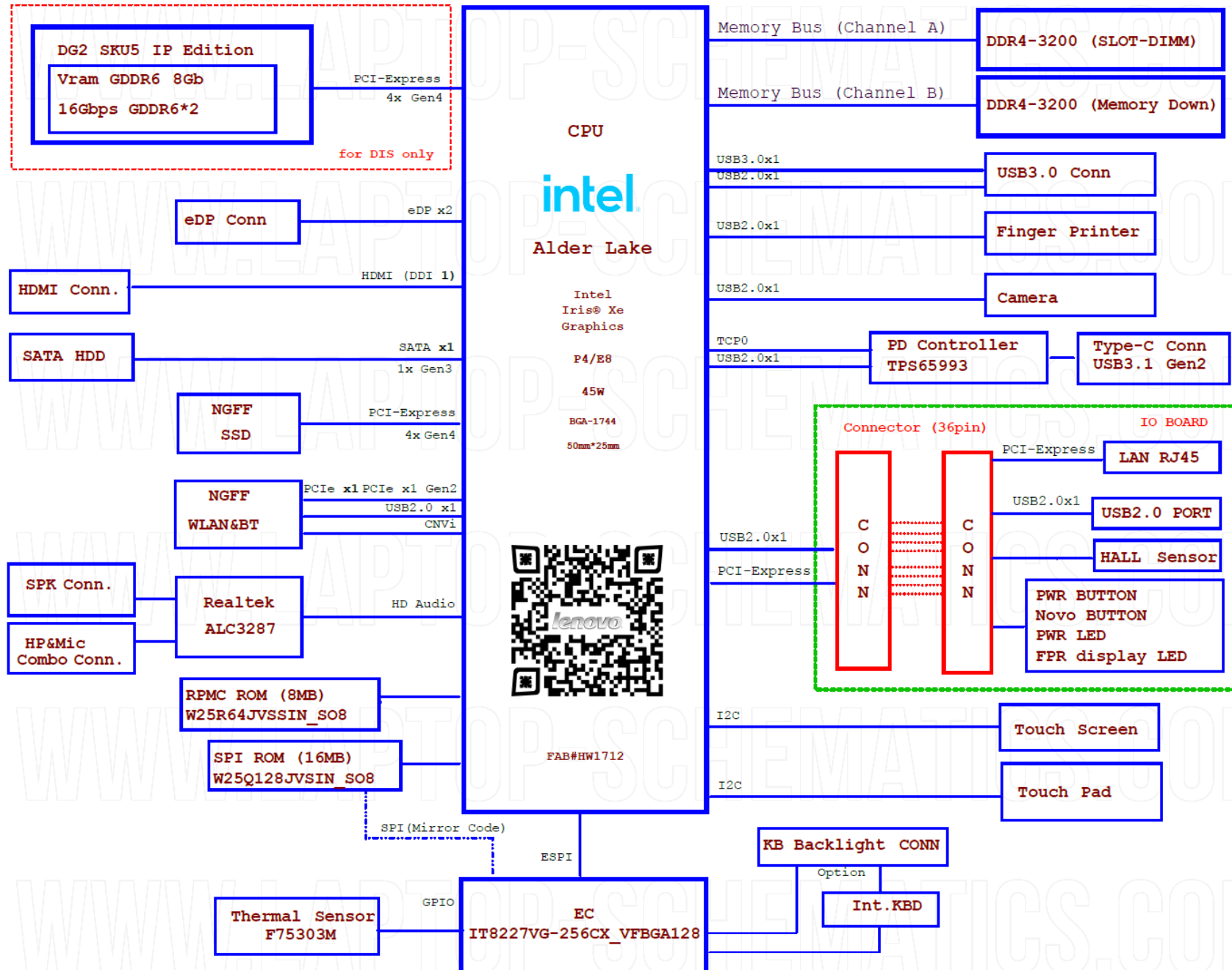
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REV : EVT

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Issued Date		Deciphered Date		Crappie e	
2012/07/01		2014/07/01		LCFC	
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				C	Cover Page
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Block Diagram



Project : Crappie_IAH

PCB # NM-XXXX
I/O BD# JV471 NS-E361 (for 14")/JV371 NS-E362 (for 15")

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Title	Crappie e	LCFC
Doc. Number	Block Diagram EE	
Date	Monday, December 05 2022	Sheet 2 of 110

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn
	2 USB3.0 Conn
	3 NC
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn
	2 NC
	3 USB3.0 Conn
	4 USB2.0 conn
	5 Card reader
	6 Touch Screen
	7 Camera
	8 NC
	9 NC
	10 Bluetooth
PCIE	5~8 X4 DGPU
	9 WLAN
	10 NC
	11 SATA HDD
	12 NC
	13~16 X4 PCIE/SATA SSD

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WIMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

EC SMBus2 address

EC SMBus3 address

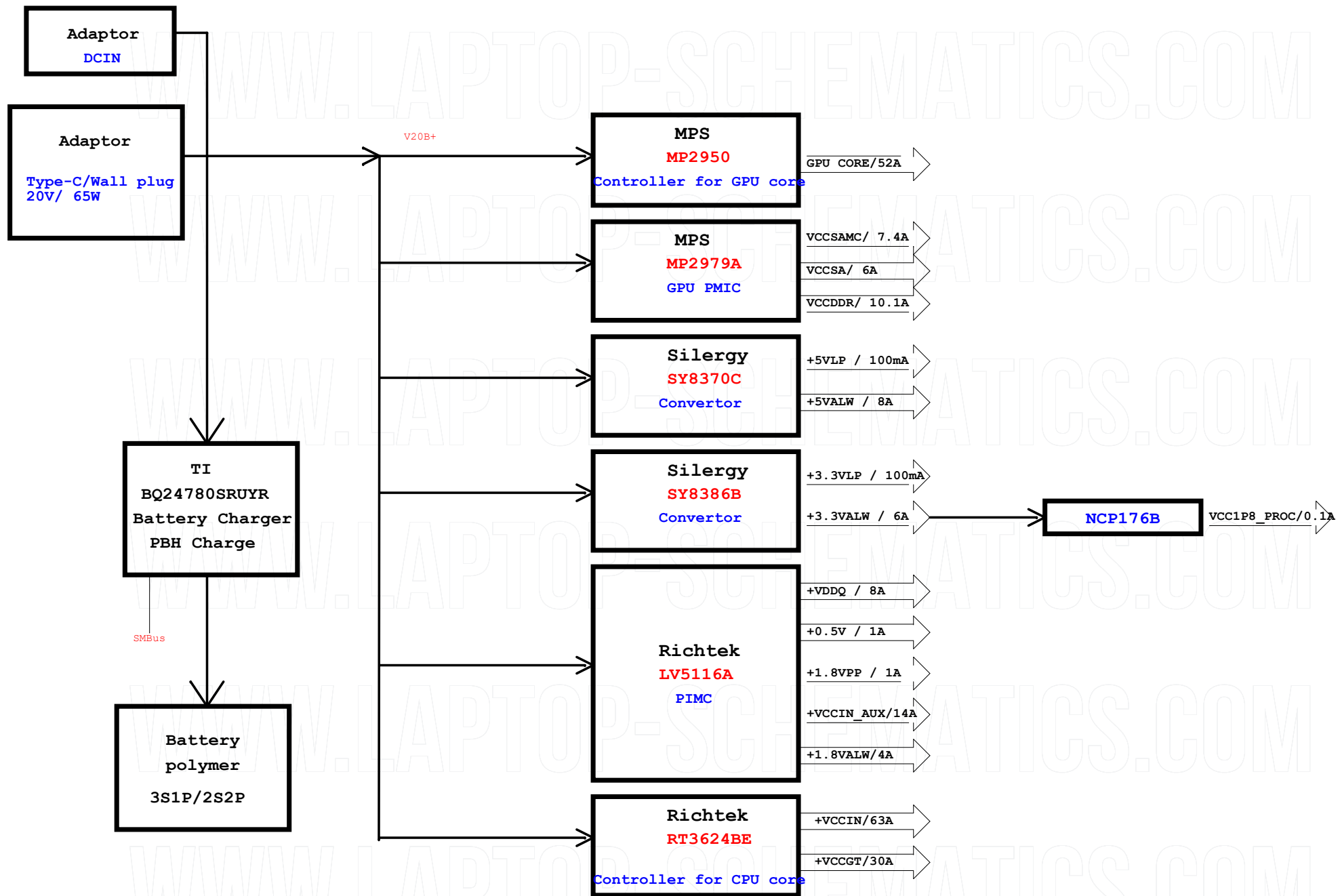
PCH SM Bus address

Device Address
Smart Battery need to update
Charger 0001 0010 b
GPU PWR Controller need to update

Device Address
Thermal Sensor(NCT7718W) 1001_100xb
PCH need to update

Device Address
not use

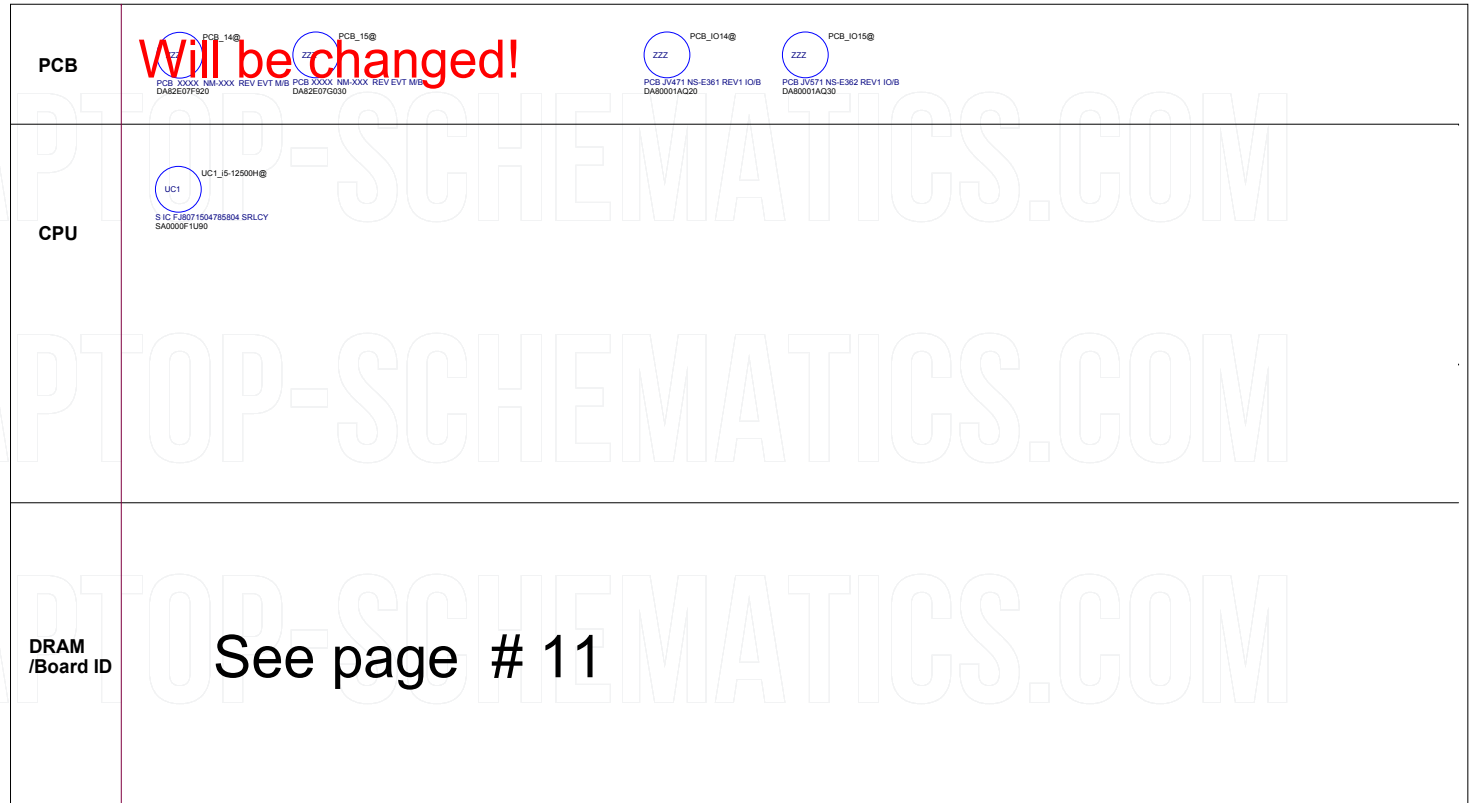
Device Address
DDR4 SODIMM need to update
WLAN Reserved
DGPU need to update

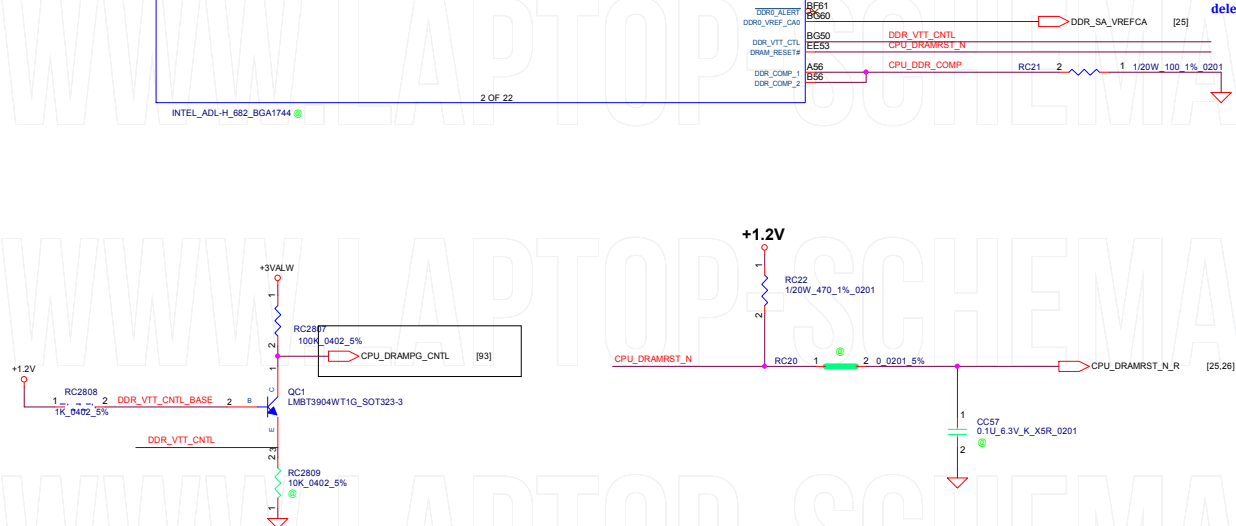
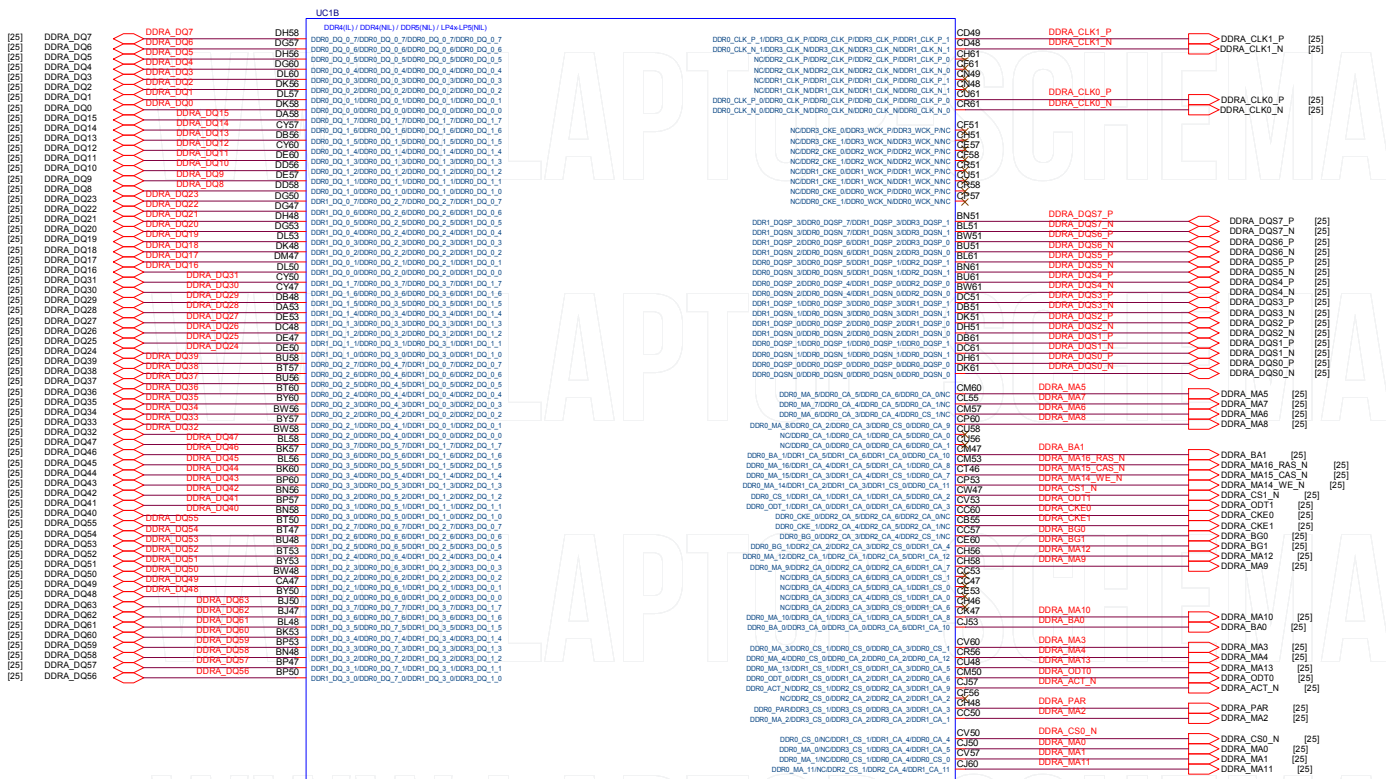


BOM Structure

BOM Structure	Description
@	Un-stuff
FHD@	For FHD Panel Part
HDR@	For HDR Panel Part
14@	For 14" part
15@	For 15" Part
17@	For 17" Part
8M_ROM@	For 8G BIOS ROM part
AMP@	For external Amplifier solution part
AMP_NS@	For external Amplifier solution un-stuff part
AMP_PWR@	For discrete Amplifier power solution part
ANS@	For power ANS solution part
USM@	For power USM solution part
BL@	For Key Board Backlight part
CD@	For C. cost down
CHANNELA@	For Memory Channel A part
DDPA@	For Memory Channel A DDP part
SDPA@	For Memory Channel A SDP part
DDPB@	For Memory Channel B DDP part
SDPB@	For Memory Channel B SDP part
NPI@	For NPI Phase part
MP@	For MP Phase Part
PCIE4@	For PCIE Gen4 part
EMC@	For EMC part
EMC_15@	For GYG51 EMC part
EMC_NS@	For EMC un-stuff part
RF_NS@	For RF Un-Stuff part
AOAC@	For AOAC part
CNVi@	For CNVi WLAN part
ME@	For ME part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For Touch Pad Part
UMA@	For UMA part

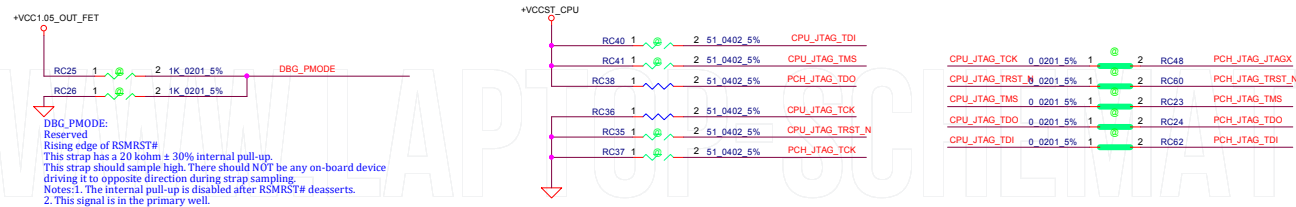
Virtual Symbol_EE





delete alert 0804

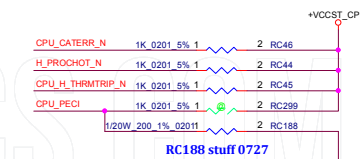
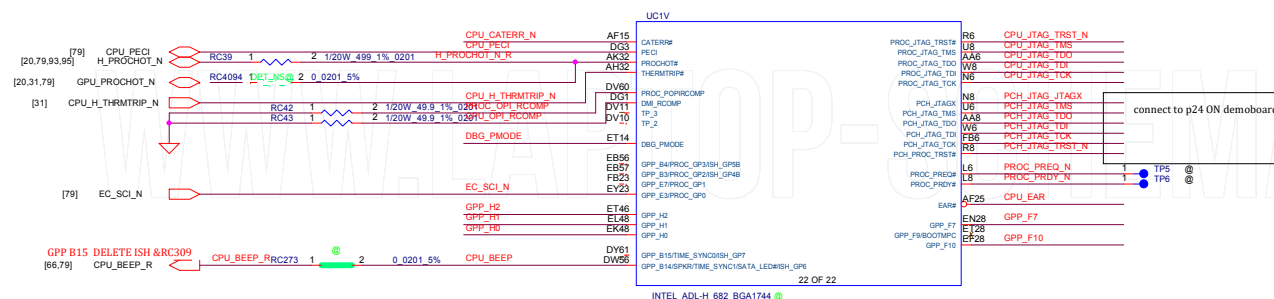
Debug usage



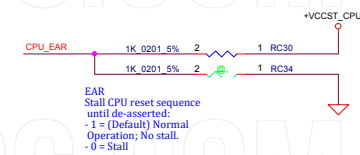
Design Notice



DELETE ISH RC308 PULL HIGH TO 3VS RSVD



RC188 stuff 0727



EAR
Stall CPU reset sequence
until de-asserted:
- 1 = (Default) Normal
Operation; No stall.
- 0 = Stall



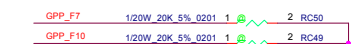
GPP A16(PCH, BEEP):
Rising edge of PCH_PWROK

The strap has a 20 kohn \pm 30% internal pull-down.

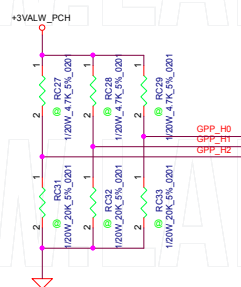
- 0 = Disable Top Swap bit. (default)
- 1 = Enable Top Swap bit. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate top swap image of the device. (boot block: PCH will invert A16 [default] for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.

Notes:

1. The internal pull-down is disabled after PCH_PWROK is high.
2. Software will not be able to clear the Top Swap bit until the system is rebooted.
3. The status of this strap is readable using the Top Swap bit (BusFwCtrl.FirmwareControl, bit4).
4. This signal is in the primary well.

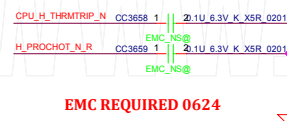


GPP_F7 and GPP_F10:
Reserved, Rising edge of RSMRST#
This strap has a 20 kohm \pm 30% internal pull-down.
This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.




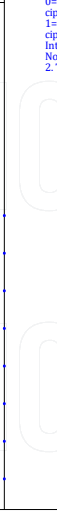
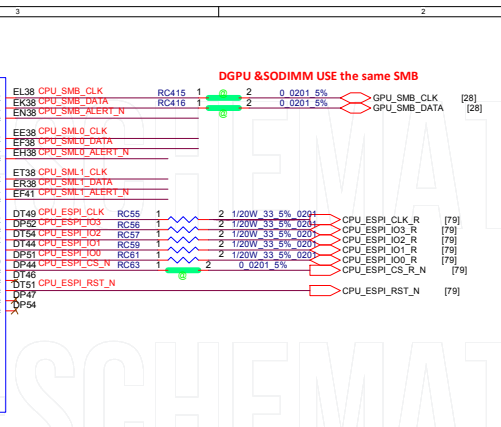
GPP_H0: Boot Strap 1
GPP_H1: Boot Strap 2
GPP_H2: Boot Strap 3
Boot Strap, Rising edge of RSMRST#
These straps has ~ 20 kohm ± 30% internal pull-down.
They bit [3:1] of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.
3. *0000 = Master Attached Flash Configuration (BIOS / CSME on SPI), eSPI is enabled
0100 = Master Attached Flash Configuration (BIOS / CSME on SPI), eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel, CSME on master attached SPI
1000 = BIOS on eSPI Peripheral Channel, CSME on master attached SPI (slave device)
1100 = BIOS on eSPI peripheral Channel, CSME on slave attached SPI.

EMC/RF Required



EMC REQUIRED 0624

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					P010-CPU(4/16) : MISC/JTAG	
Date:				Monday, December 05, 2022	Sheet	10 of 110



Board ID Table 1: 1.8V Level				
Board ID10	GPP_F13 H			
Board ID11	GPP_F14 L			
Board ID12	GPP_F15 H	00	UMA	***
		01	DIS-SAM	***
Board ID13	GPP_F16 L	10	DIS-HYX	***
		11		***
Board ID14	GPP_F17	00	S170	***
		01	S370	***
Board ID15	GPP_F18	10	V14V15	***
		11	S14S15	***

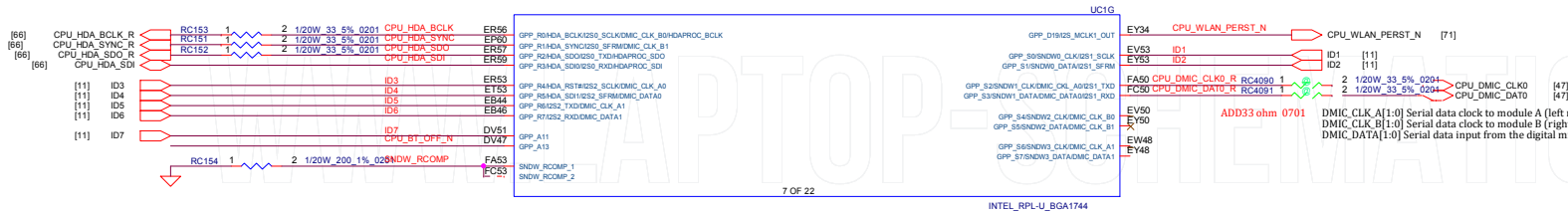
The diagram illustrates a cryptographic hardware configuration, likely for a Crappie processor. It features a grid of components connected to a set of 16 input/output lines (ID1-ID16) and a set of 16 control lines (ID1-ID16). The components include various logic gates (AND, OR, NOT, XOR, XNOR), multiplexers (MUX), and registers (RC). The diagram is labeled with 'LCFC' and 'Crappie'.

Legend:

- RC103: 100K_0001_5%
- RC104: 100K_0001_5%
- RC105: 100K_0001_5%
- RC106: 100K_0001_5%
- RC107: 100K_0001_5%
- RC108: 100K_0001_5%
- RC109: 100K_0001_5%
- RC110: 100K_0001_5%
- RC111: 100K_0001_5%
- RC112: 100K_0001_5%
- RC113: 100K_0001_5%
- RC114: 100K_0001_5%
- RC115: 100K_0001_5%
- RC116: 100K_0001_5%
- RC117: 100K_0001_5%
- RC118: 100K_0001_5%
- RC119: 100K_0001_5%
- RC120: 100K_0001_5%
- RC121: 100K_0001_5%
- RC122: 100K_0001_5%
- RC123: 100K_0001_5%
- RC124: 100K_0001_5%
- RC125: 100K_0001_5%
- RC126: 100K_0001_5%
- RC127: 100K_0001_5%
- RC128: 100K_0001_5%
- RC129: 100K_0001_5%
- RC130: 100K_0001_5%
- RC131: 100K_0001_5%
- RC132: 100K_0001_5%
- RC133: 100K_0001_5%
- RC134: 100K_0001_5%
- RC135: 100K_0001_5%
- RC136: 100K_0001_5%
- RC137: 100K_0001_5%
- RC138: 100K_0001_5%
- RC139: 100K_0001_5%
- RC140: 100K_0001_5%
- RC141: 100K_0001_5%
- RC142: 100K_0001_5%
- RC143: 100K_0001_5%
- RC144: 100K_0001_5%
- RC145: 100K_0001_5%
- RC146: 100K_0001_5%
- RC147: 100K_0001_5%
- RC148: 100K_0001_5%
- RC149: 100K_0001_5%
- RC150: 100K_0001_5%
- RC151: 100K_0001_5%
- RC152: 100K_0001_5%
- RC153: 100K_0001_5%
- RC154: 100K_0001_5%
- RC155: 100K_0001_5%
- RC156: 100K_0001_5%
- RC157: 100K_0001_5%
- RC158: 100K_0001_5%
- RC159: 100K_0001_5%
- RC160: 100K_0001_5%
- RC161: 100K_0001_5%
- RC162: 100K_0001_5%
- RC163: 100K_0001_5%
- RC164: 100K_0001_5%
- RC165: 100K_0001_5%
- RC166: 100K_0001_5%
- RC167: 100K_0001_5%
- RC168: 100K_0001_5%
- RC169: 100K_0001_5%
- RC170: 100K_0001_5%
- RC171: 100K_0001_5%
- RC172: 100K_0001_5%
- RC173: 100K_0001_5%
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- RC184: 100K_0001_5%
- RC185: 100K_0001_5%
- RC186: 100K_0001_5%
- RC187: 100K_0001_5%
- RC188: 100K_0001_5%
- RC189: 100K_0001_5%
- RC190: 100K_0001_5%
- RC191: 100K_0001_5%
- RC192: 100K_0001_5%
- RC193: 100K_0001_5%
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- RC197: 100K_0001_5%
- RC198: 100K_0001_5%
- RC199: 100K_0001_5%
- RC200: 100K_0001_5%
- RC201: 100K_0001_5%
- RC202: 100K_0001_5%
- RC203: 100K_0001_5%
- RC204: 100K_0001_5%
- RC205: 100K_0001_5%
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- RC210: 100K_0001_5%
- RC211: 100K_0001_5%
- RC212: 100K_0001_5%
- RC213: 100K_0001_5%
- RC214: 100K_0001_5%
- RC215: 100K_0001_5%
- RC216: 100K_0001_5%
- RC217: 100K_0001_5%
- RC218: 100K_0001_5%
- RC219: 100K_0001_5%
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- RC226: 100K_0001_5%
- RC227: 100K_0001_5%
- RC228: 100K_0001_5%
- RC229: 100K_0001_5%
- RC230: 100K_0001_5%
- RC231: 100K_0001_5%
- RC232: 100K_0001_5%
- RC233: 100K_0001_5%
- RC234: 100K_0001_5%
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- RC253: 100K_0001_5%
- RC254: 100K_0001_5%
- RC255: 100K_0001_5%
- RC256: 100K_0001_5%
- RC257: 100K_0001_5%
- RC258: 100K_0001_5%
- RC259: 100K_0001_5%
- RC260: 100K_0001_5%
- RC261: 100K_0001_5%
- RC262: 100K_0001_5%
- RC263: 100K_0001_5%
- RC264: 100K_0001_5%
- RC265: 100K_0001_5%
- RC266: 100K_0001_5%
- RC267: 100K_0001_5%
- RC268: 100K_0001_5%
- RC269: 100K_0001_5%
- RC270: 100K_0001_5%
-

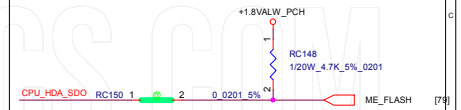
[illegible]

pay attion to this id3,
connect to the unused id better



Design Notice

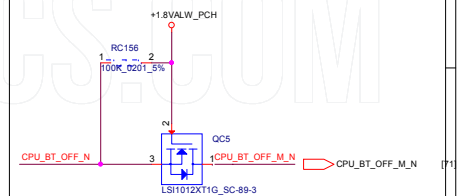
DMIC_CLK_A[1:0] Serial data clock to module A (left microphone) DMIC on interface/port 0 or 1.
DMIC_CLK_B[1:0] Serial data clock to module B (right microphone) DMIC on interface/port 0 or 1.
DMIC_DATA[1:0] Serial data input from the digital microphone module



GPP_R2(PCH_HDA_SDO):
Flash Descriptor Security Override
Rising edge of PCH_PWROK
This strap has a 20 kohm \pm 30% internal pull-down.
0 -> Enable security measures defined in the Flash Descriptor (Default)
1 -> Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.
Notes: 1. The internal pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

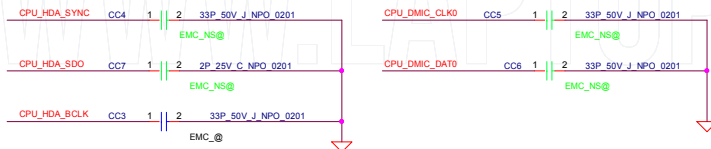


Glitch Free Recommended:
Site for pull-down resistor only.



Signal: CPU_BT_OFF_M_N
Voltage Level: 1.8V
LSI012XT1G_SC-89-3
Vds max=20V
Vgs max=+/- 6V
Vgs(th)=0.45V(0.9V(min/max))
Ids(ON)=1.250mA(max, Vgs=1.8V)
Id=350mA(TA=25 C)
Ton Delay=5ns
Rise Time=5ns

EMC/RF Required



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Title		Crappie e		LCFC	
Document Number	P013-CPU(7/16) : AUDIO	Rev	EVT		
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**Card Reader
OR LAN**




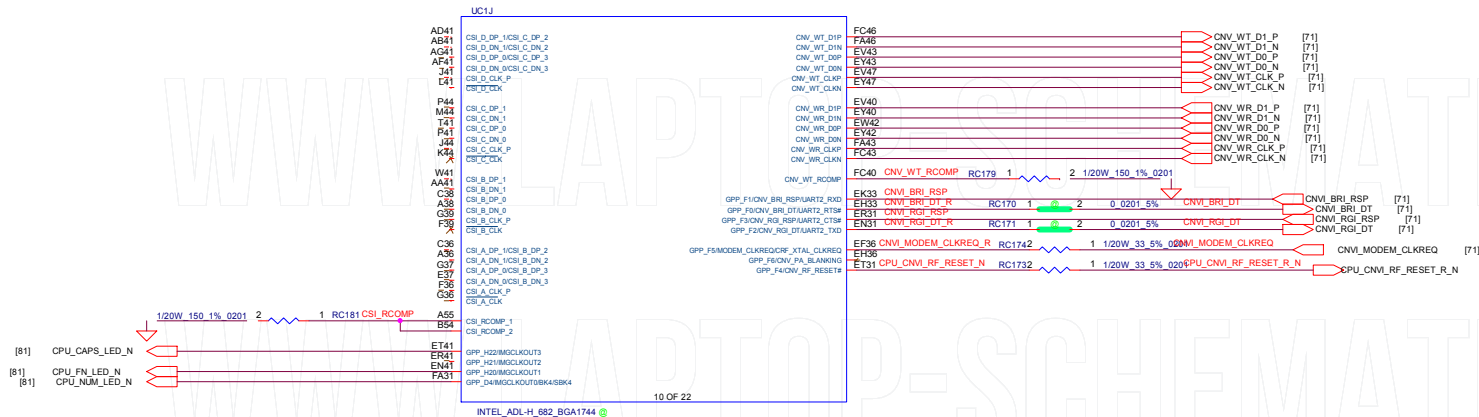
USB_OC3_N RC271 1 2 10K_0201_5%

RC163 pull high to +3VALW_PCH 0624

GPU [28] P
[28] P
[28] P

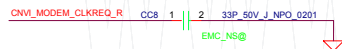


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Size		Document Number					Rev
		P014-CPU(8/16) : PCIE/USB/SATA					1.0
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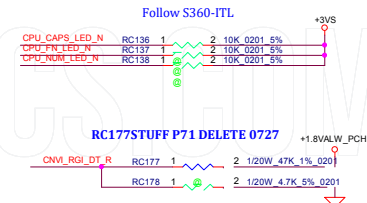


the diffrent with Base:
1.C970 Use GPP_D4 FOR UART_BT_WAKE,S170 no USE

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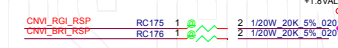
Design Notice



GPP_F2 / CNV_RGL_DT / UART2_TXD:
M2 CNVI MODES, Rising edge of RSMRST#
This strap does not have an internal pull-up or pull-down.
A weak external pull-up is required.
0 = Integrated CNVI enabled.
1 = Integrated CNVI disabled.
Note: When a RF companion chip is connected to the PCH CNVI interface, the device internal pulldown resistor will pull the strap low to enable CNVI interface.

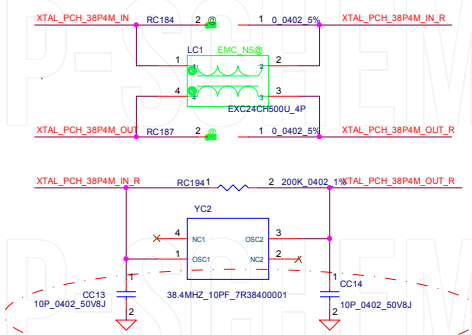
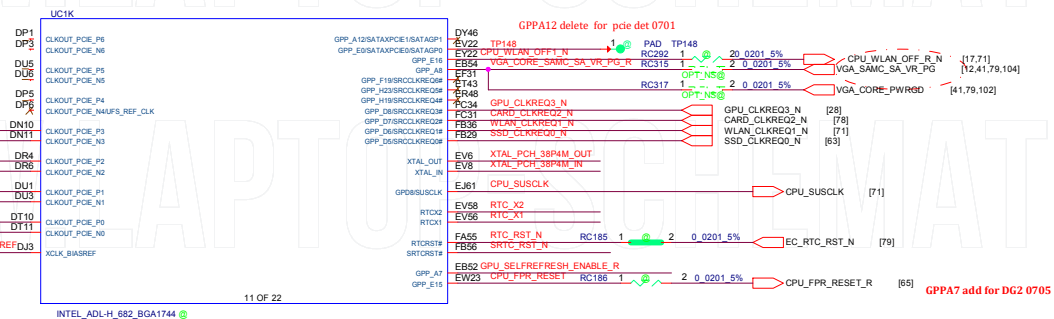
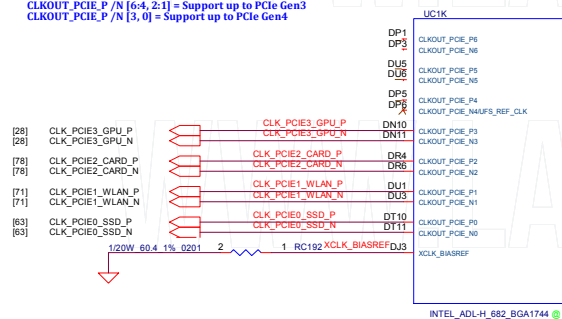


GPP_F0 / CNV_BRI_DT / UART2_RTS#
XTAL Frequency Selection, Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
This strap should not be pulled high since 24 MHz crystal is not supported on the PCH.
0 = 38.4 MHz (default)
1 = 24 MHz
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

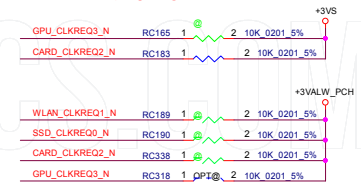


Glitch Free Requirements:
Pull-down resistor to ensure the stability of the signal during platform bootup

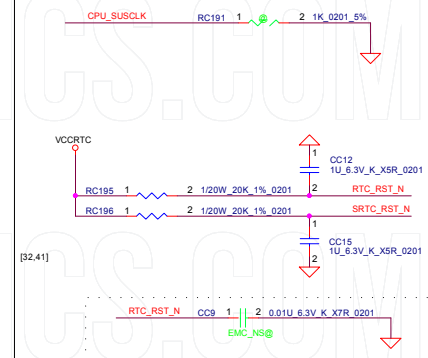


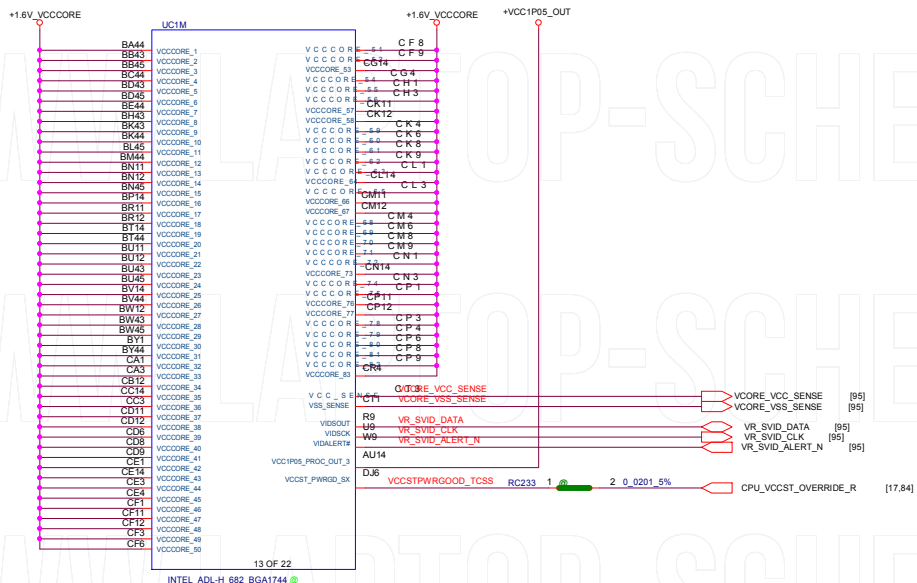


GPU_CLKREQ3_N pull high to 3VS or 3VALW_PCH?

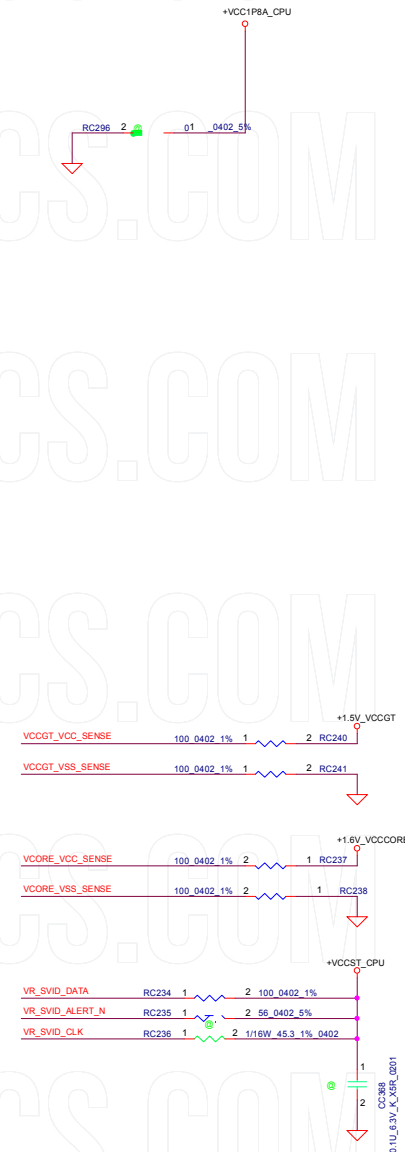


ADD RC338 RC318 0727

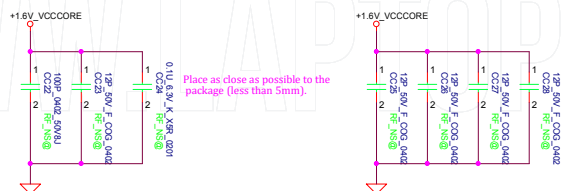




Design Notice



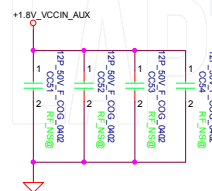
EMC/RF Required




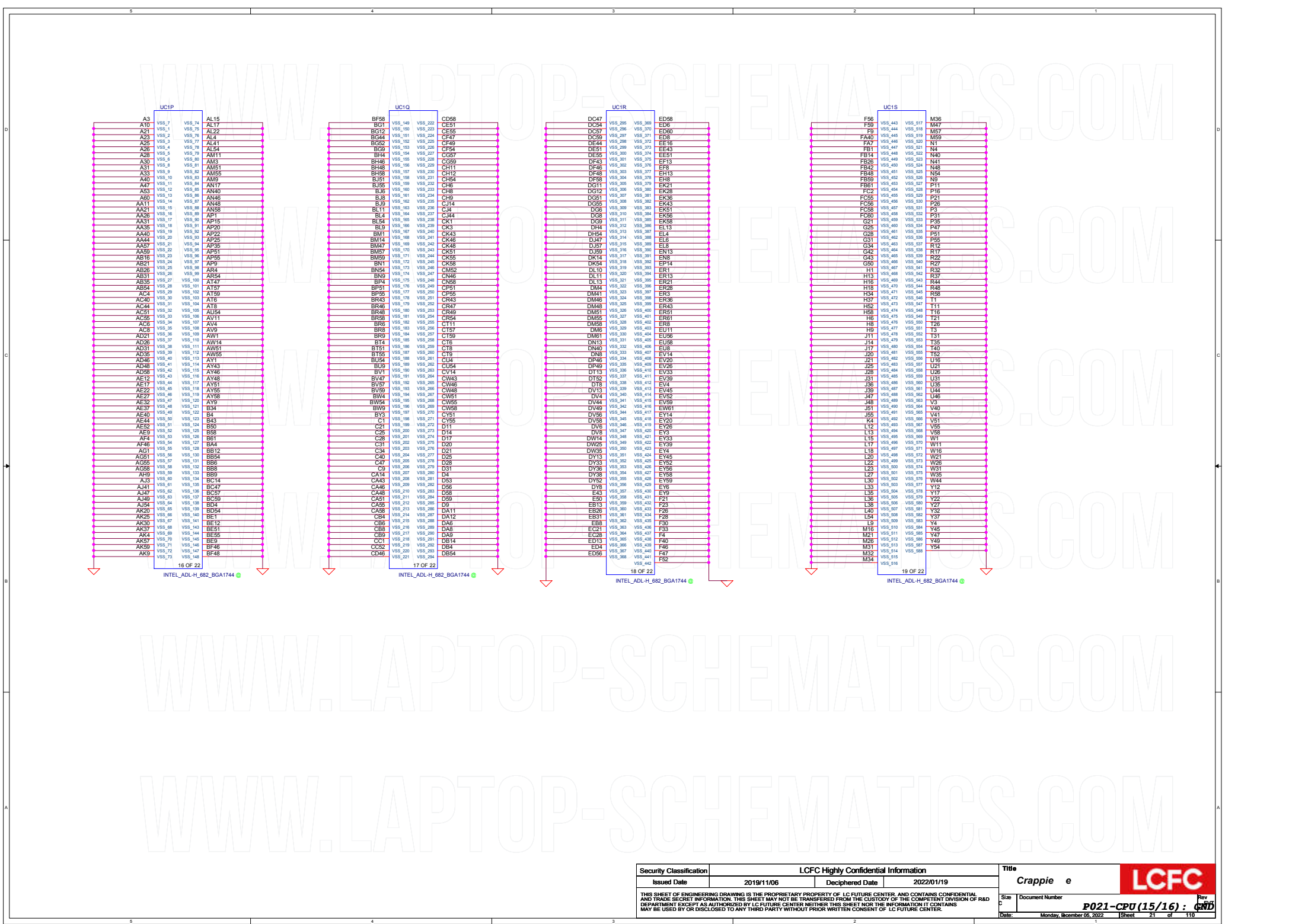
1.5VCCGT ADD RF C?

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Size		Document Number		Rev	
		P018-CPU(12/16):CPU Power(1/2)		1/2	
Date		Monday, December 05, 2022		Sheet 18 of 110	

5		4		3		2		1	
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Date				2019/11/06/2022/01/19 : Sheet 1 of 1			



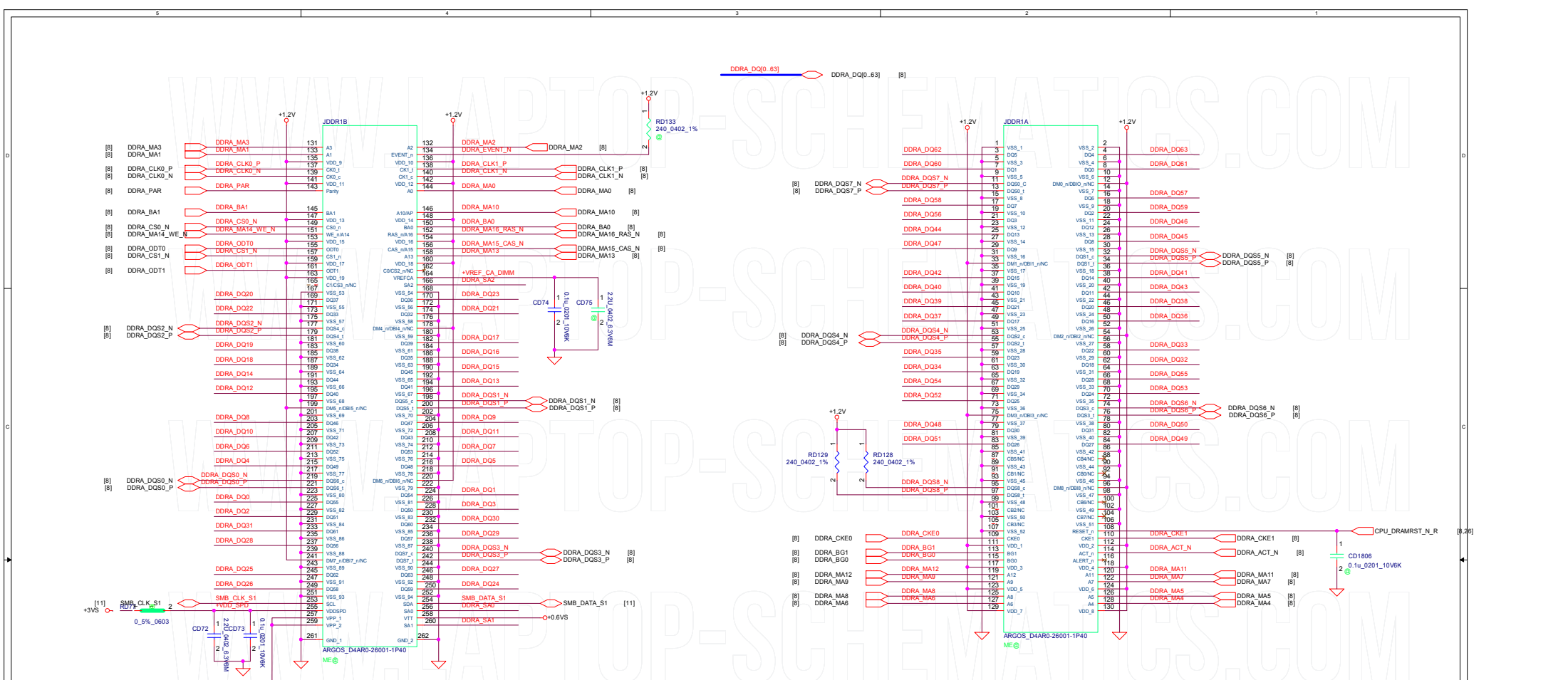
UC10

AF27
AH20
AK22
AK40
AL30
AL40
BG47
BG53
DT42
EE46
EF33
EH41

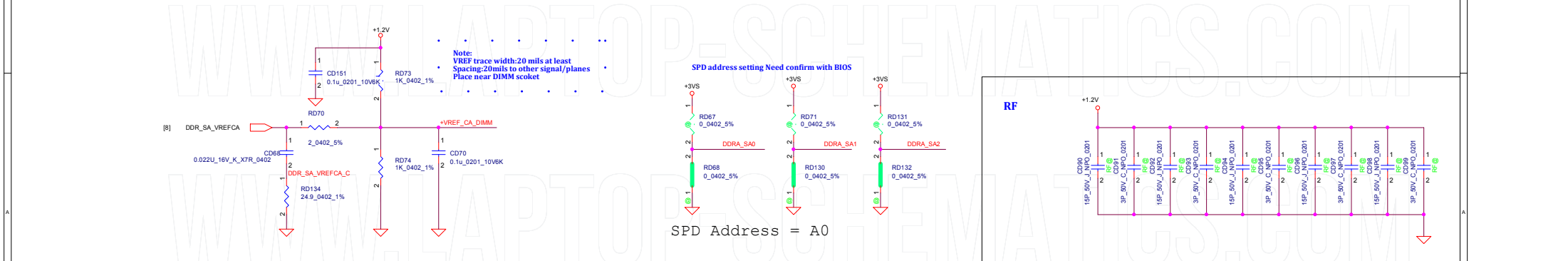
REV'D_1
REV'D_2
REV'D_4
REV'D_5
REV'D_7
REV'D_8
REV'D_9
REV'D_10
REV'D_13
REV'D_15
REV'D_16
REV'D_20

4 OF 22


INTEL_ADL-H_582_BGA1744



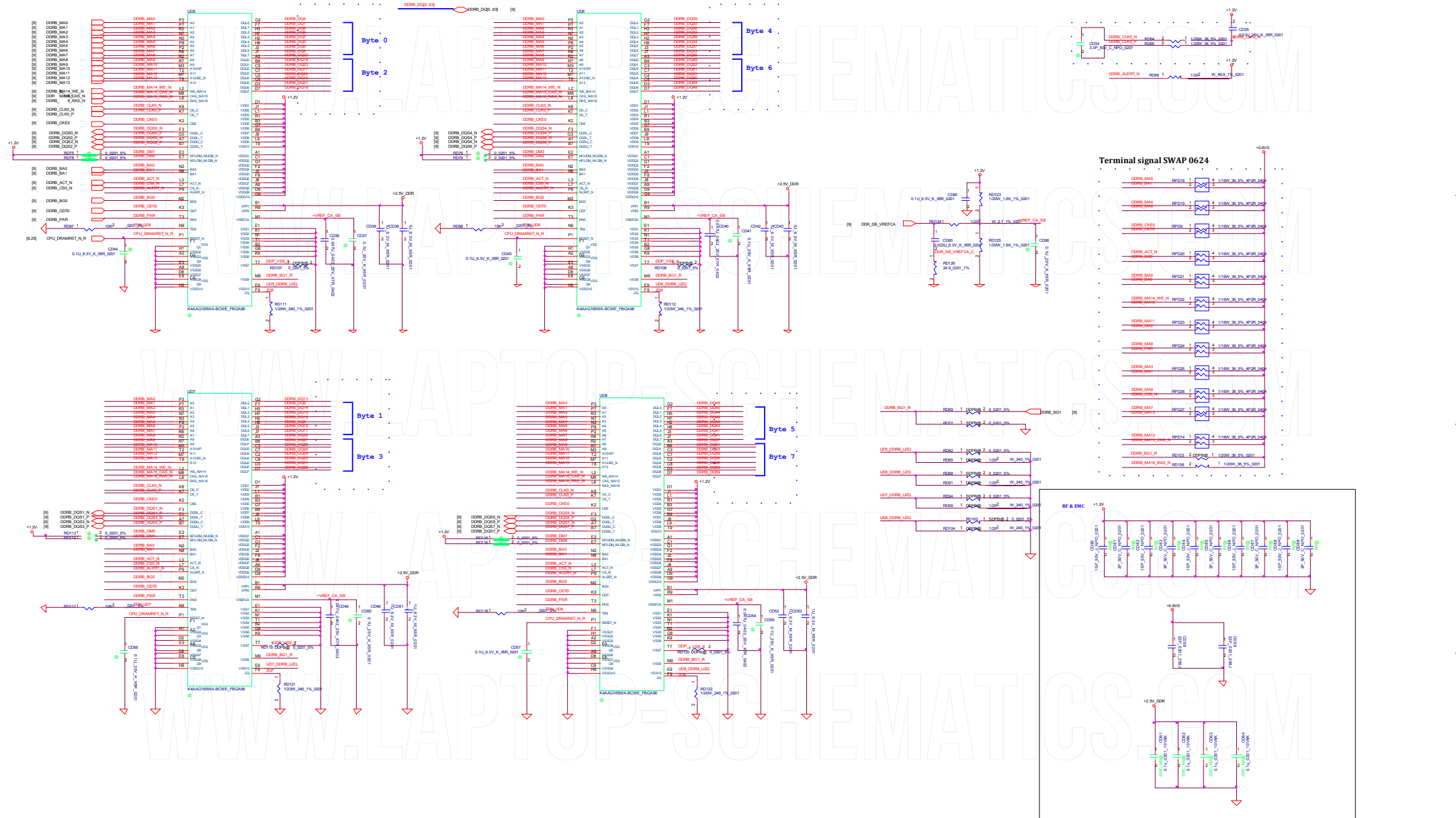
the diffrent with Base:
1.S370&V14V15 CHANNEL A use DIMM



SPD Address = A0

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Size		Document Number		Memory_CHA				Rev	
								0.1	
Date:		Monday, December 05, 2022				Sheet		25 of 110	

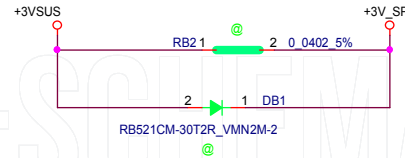
Apply X76 BOM to control SDP Memory Down stuff components!



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Document Number	Memory_CBB				
Revision	1				

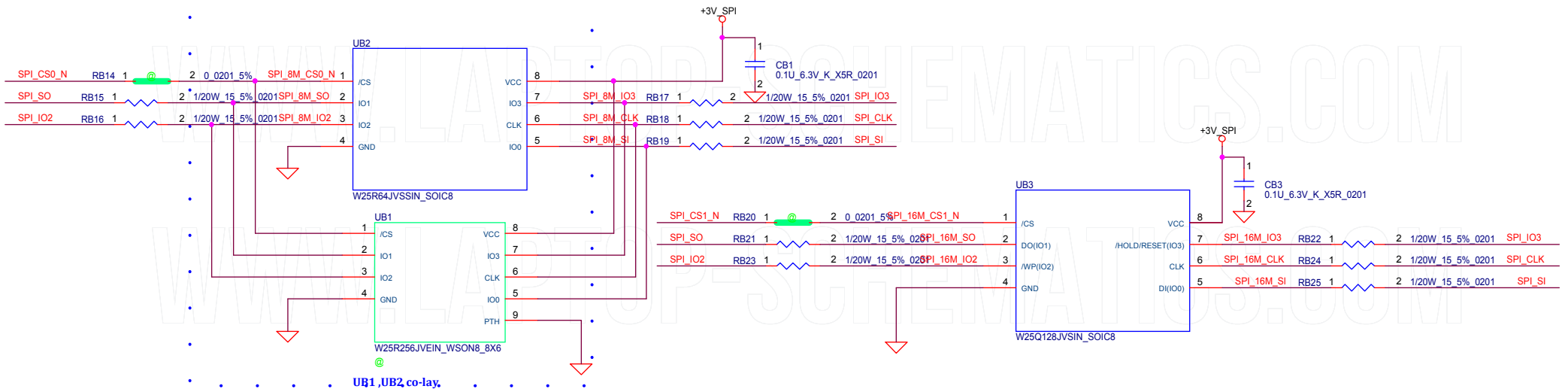
RB3,4,5,6,8CHANGE TO 00HM

[11]	CPU_SPI0_CS0_N	CPU_SPI0_CS0_N	RB1	1	2	0	0201	5%	SPI_CS0_N
[11]	CPU_SPI0_CLK	CPU_SPI0_CLK	RB8	1	2	0	0201	5%	SPI_CLK
[11]	CPU_SPI0_SI	CPU_SPI0_SI	RB3	1	2	0	0201	5%	SPI_SI
[11]	CPU_SPI0_SO	CPU_SPI0_SO	RB6	1	2	0	0201	5%	SPI_SO
[11]	CPU_SPI0_IO2	CPU_SPI0_IO2	RB4	1	2	0	0201	5%	SPI_IO2
[11]	CPU_SPI0_IO3	CPU_SPI0_IO3	RB5	1	2	0	0201	5%	SPI_IO3



[27,79]	EC_SPI_CS0_N	EC_SPI_CS0_N	RB13	1	2	0	0201	5%	SPI_CS0_N
[79]	EC_SPI_CLK	EC_SPI_CLK	RB10	1	2	1/20W	100	1% 0201	SPI_CLK
[79]	EC_SPI_SI	EC_SPI_SI	RB11	1	2	1/20W	100	1% 0201	SPI_SI
[79]	EC_SPI_SO	EC_SPI_SO	RB12	1	2	1/20W	100	1% 0201	SPI_SO

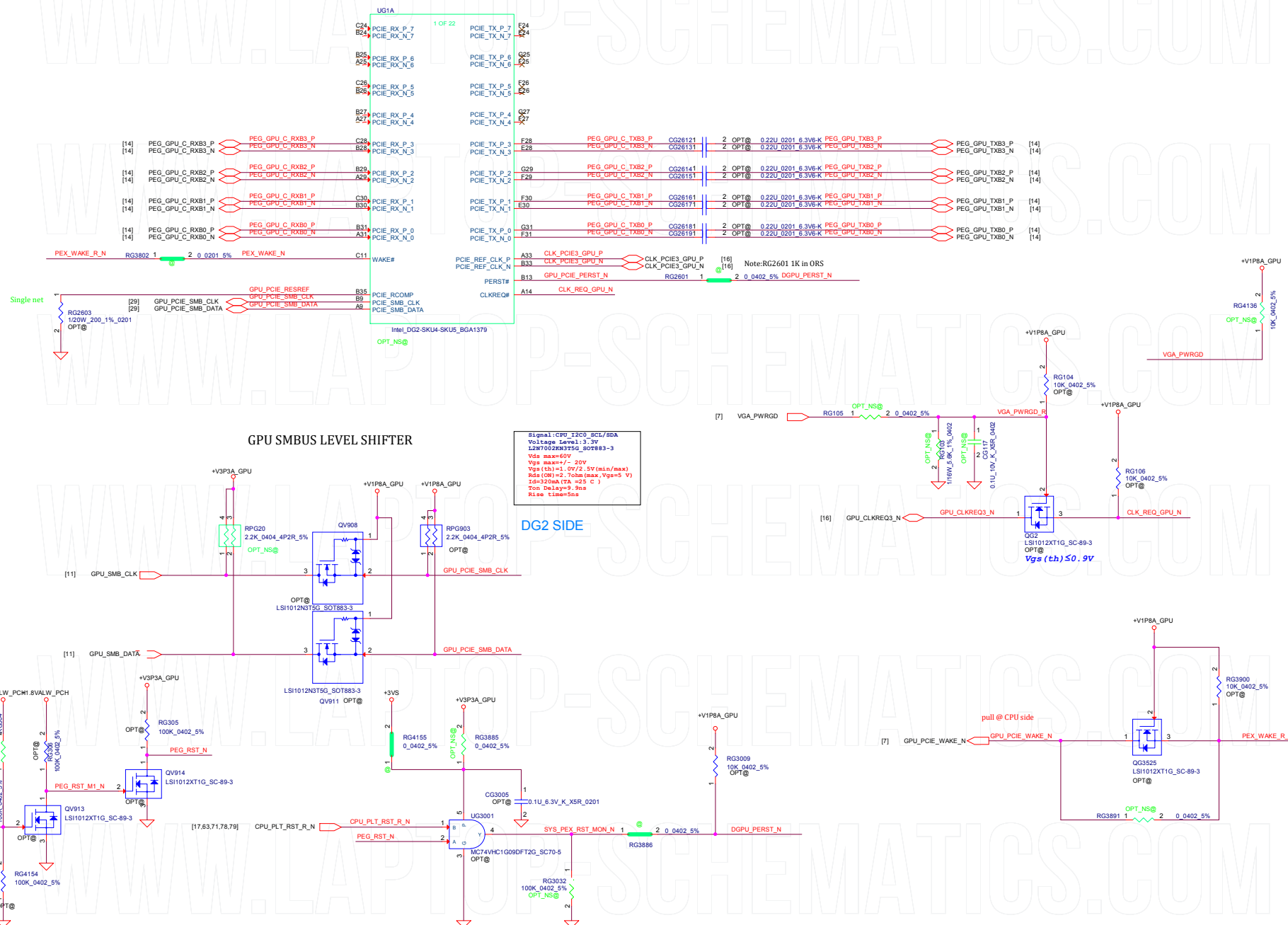
[27,79]	EC_SPI_CS0_N	RB26	1	2	0	0201	5%	SPI_CS1_N
[11]	CPU_SPI0_CS1_N	RB9	1	2	0	0201	5%	SPI_CS1_N



UB2 UB3 are changed FROM IQ to IN by common pool

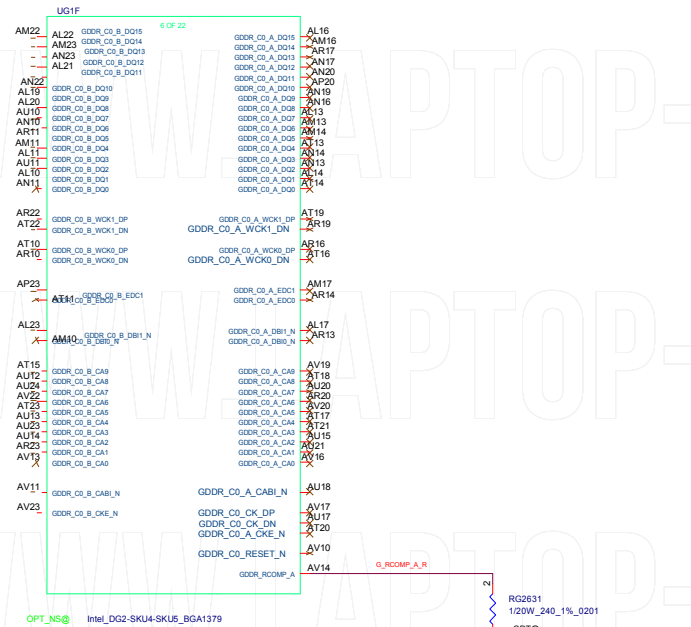
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Size B		Document Number SPI ROM/TPM								Rev 0.1	
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PCIE INTERFACE X4

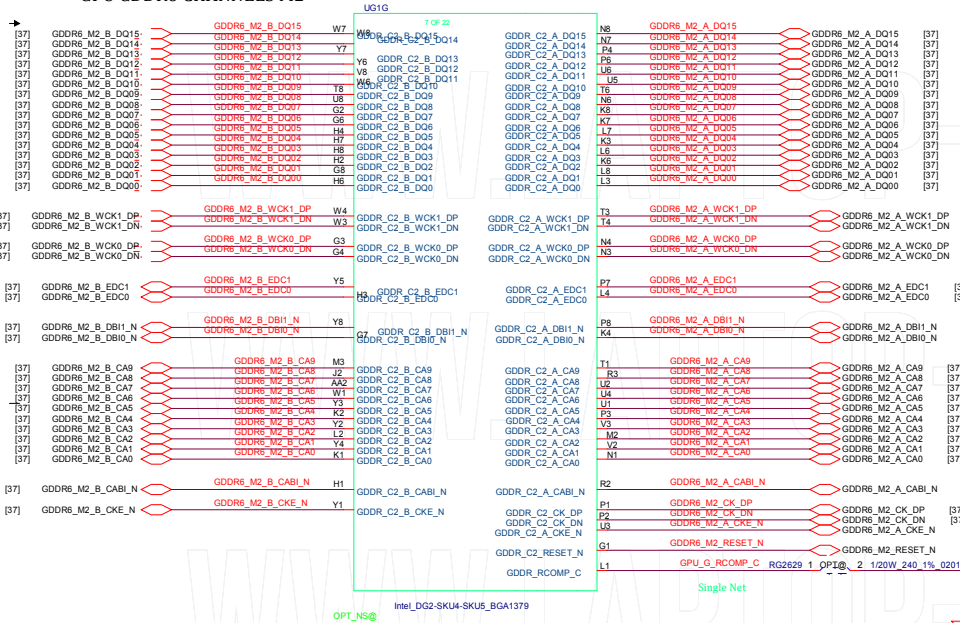


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Doc No		Document Number			
		P028-GPU PCIE Interface			
Date:		Monday, December 12, 2022			
		Sheet 28 of 113			

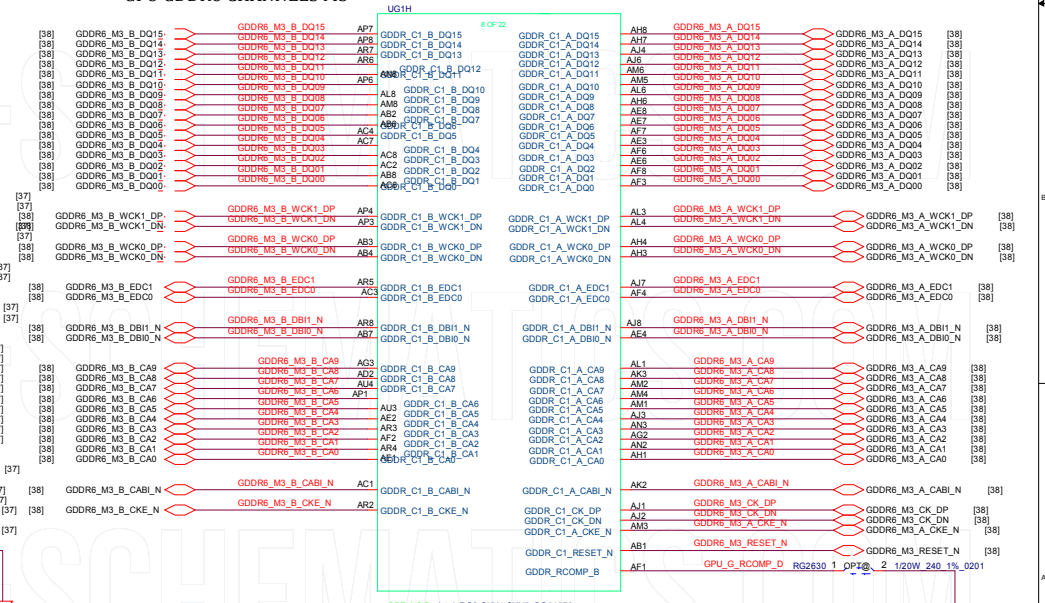
GPU GDDR6 CHANNELS M1



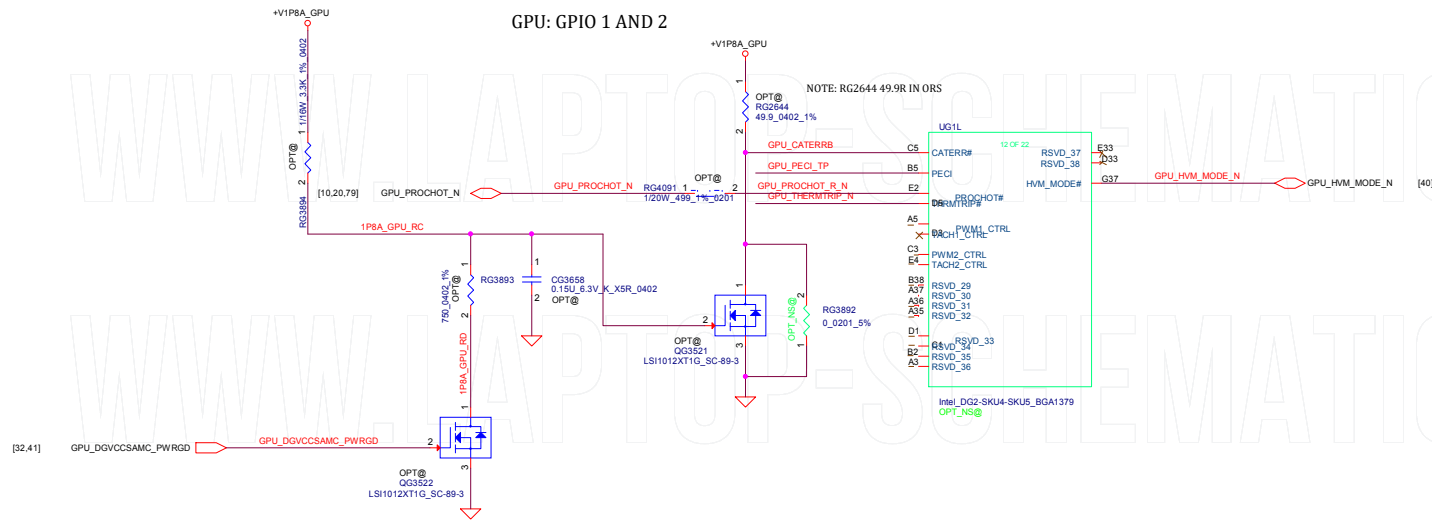
GPU GDDR6 CHANNELS M2



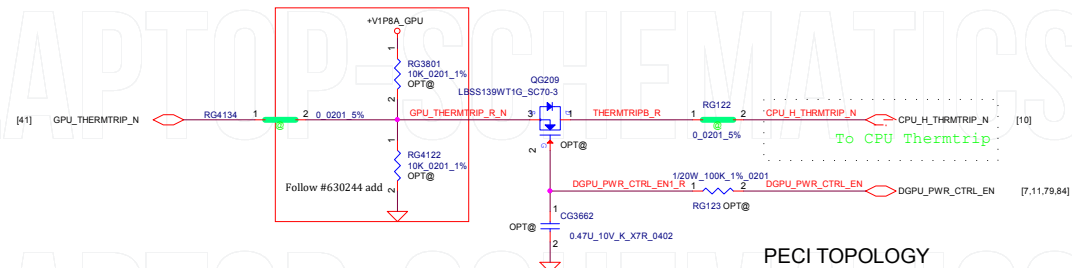
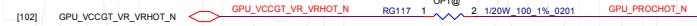
GPU GDDR6 CHANNELS M3



GPU: GPIO 1 AND 2

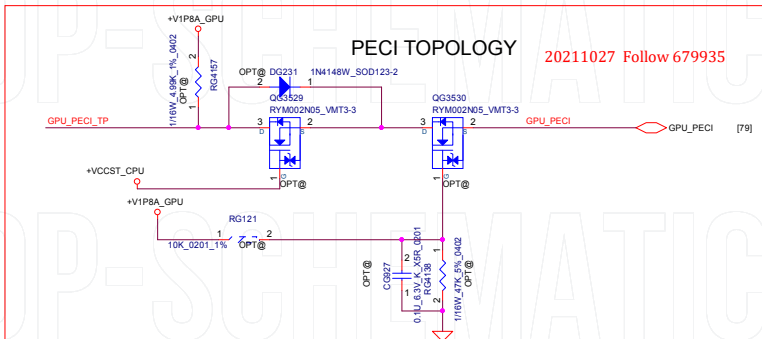


NEW ADD FOLLOW 630244

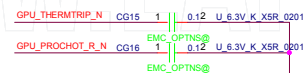


PECI TOPOLOGY

20211027 Follow 679935



EMC/RF Required



EMC REQUIRED 0624

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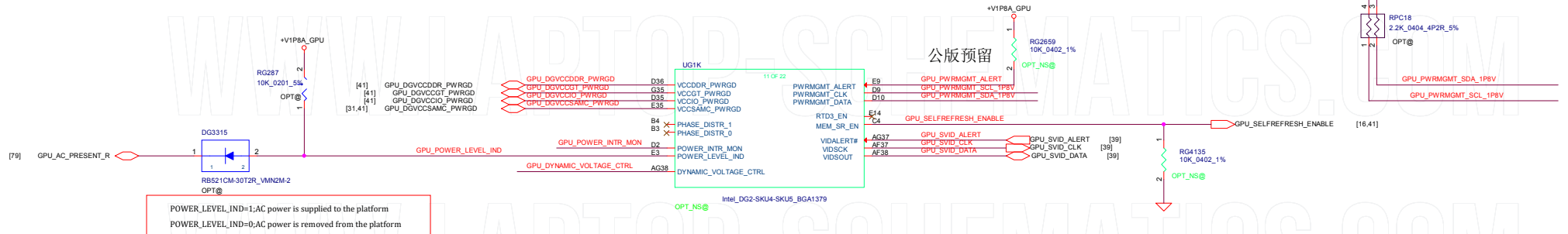
P031-GPU MEM Interface (C/D)

Date: Monday, December 12, 2022

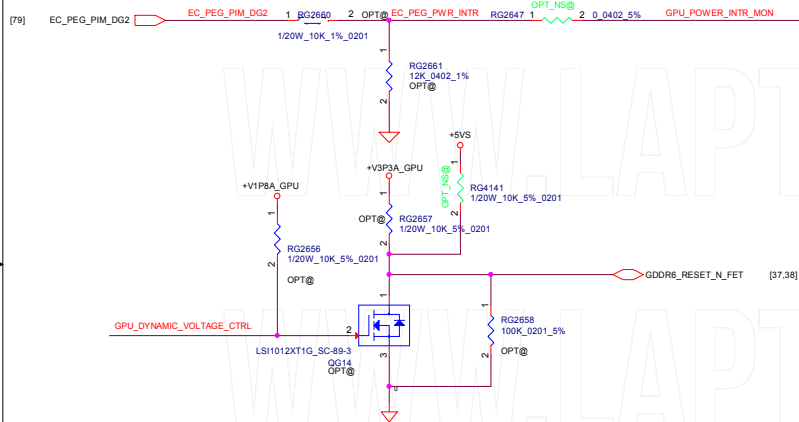
Sheet 31 of 113

Rev

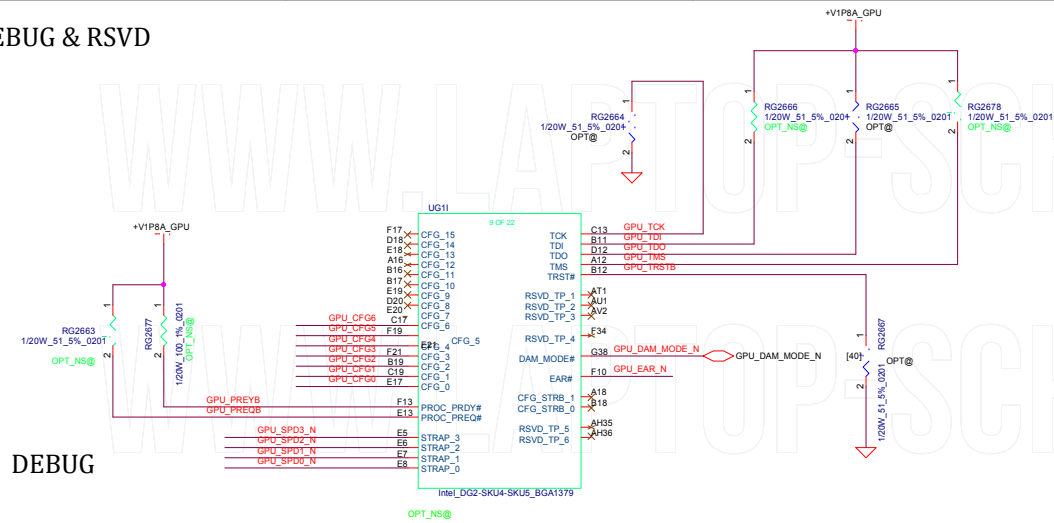
GPU: GPIO 1 AND 2



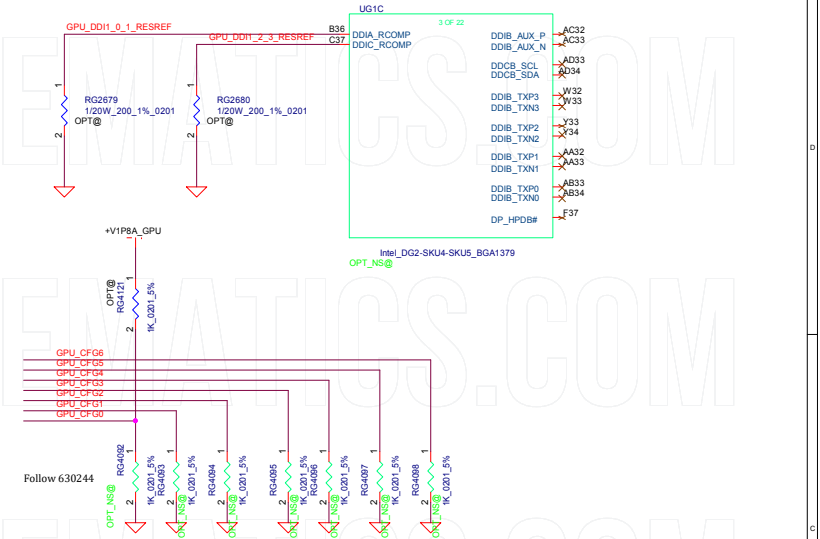
NEED CONNECTED TO EC GPIO



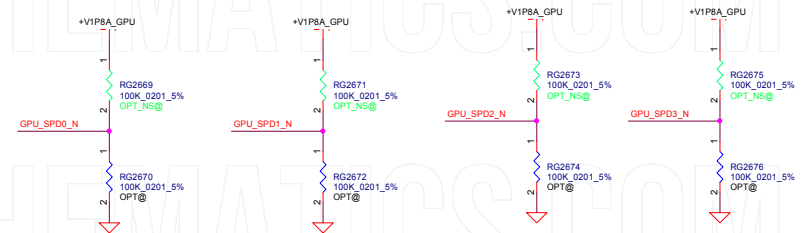
GPU: DEBUG & RSVD



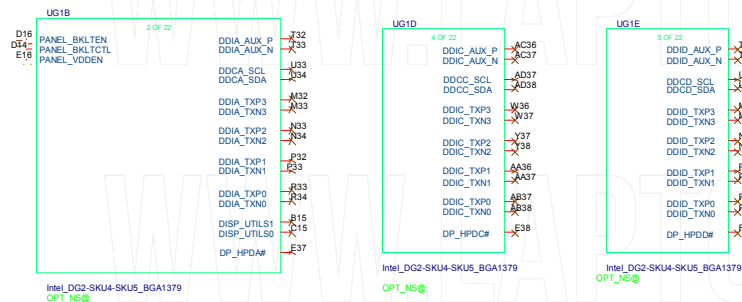
GPU DDI:B




BOARD IDENTIFICATION FOR DG2 FIRMWARE

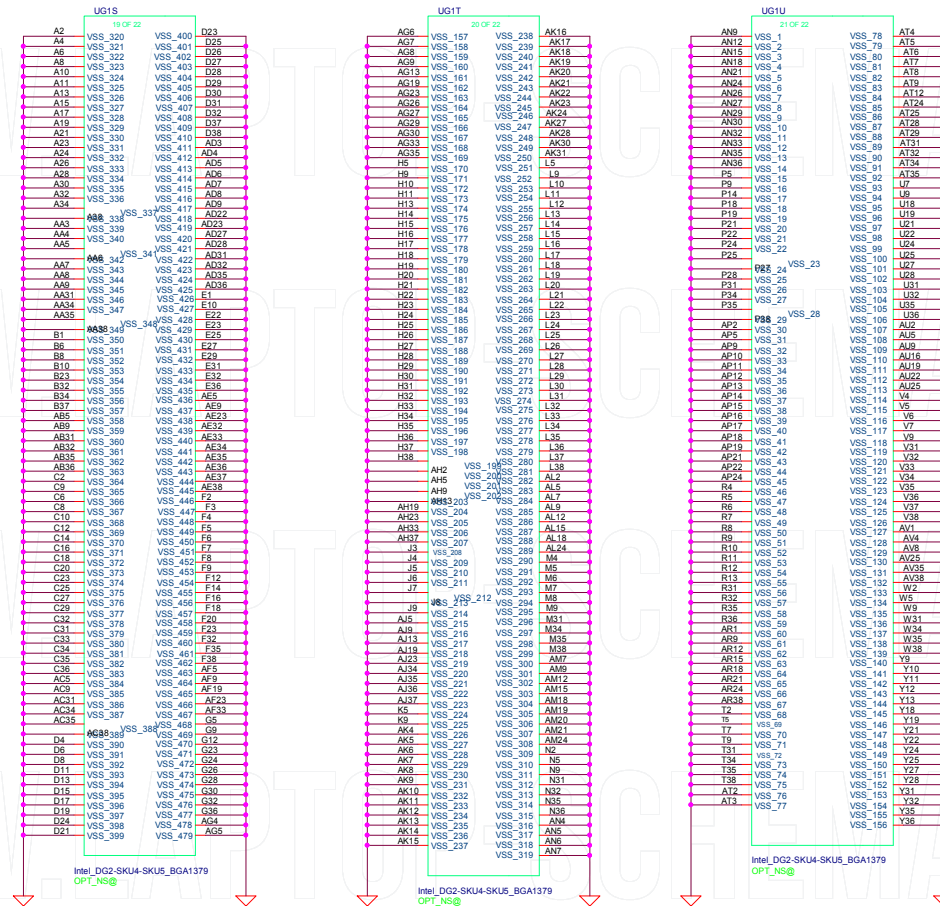


GPU DDI: A,C,D

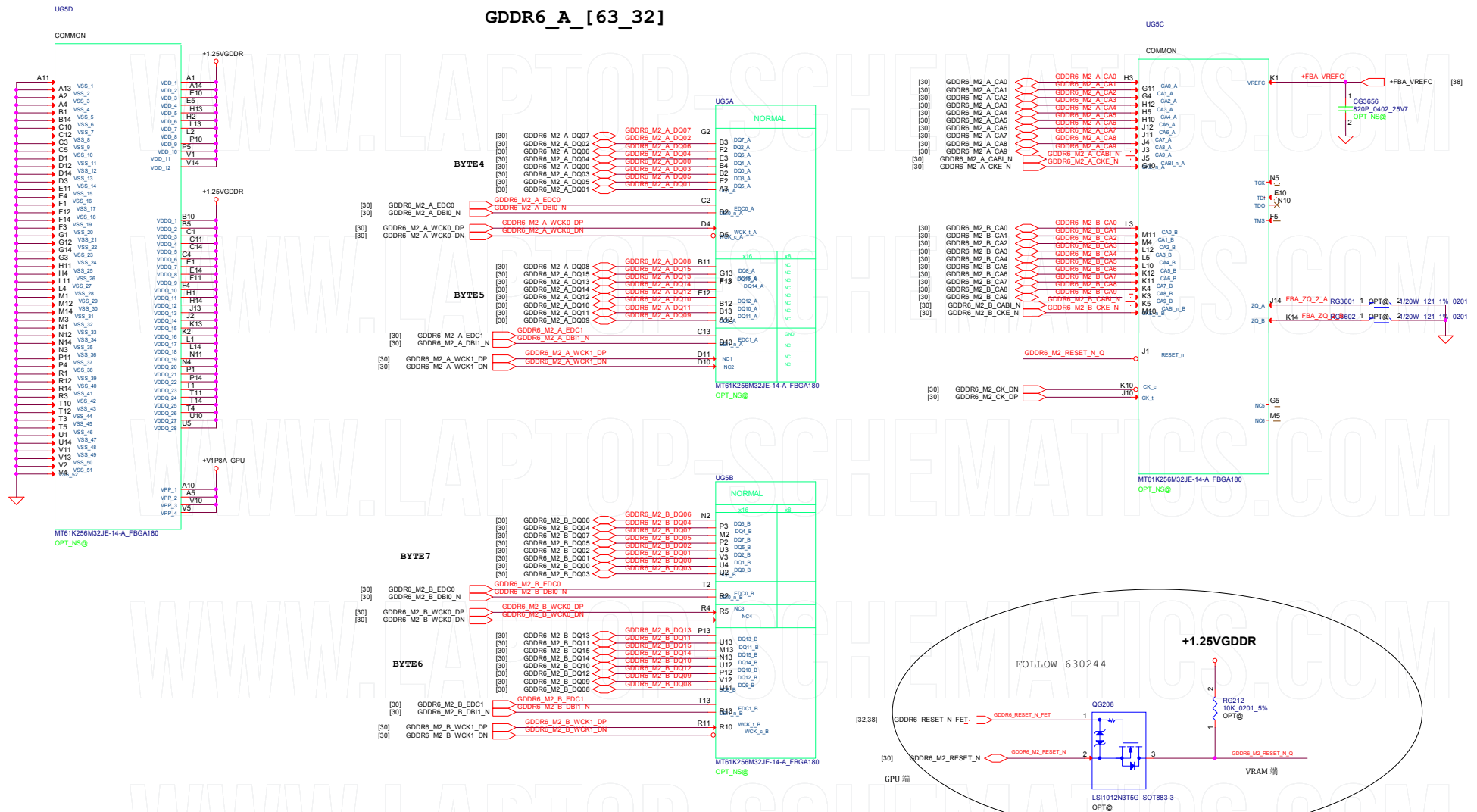


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Date:	Monday, December 12 2022			Sheet	33	of 113	

GPU POWER: GROUND

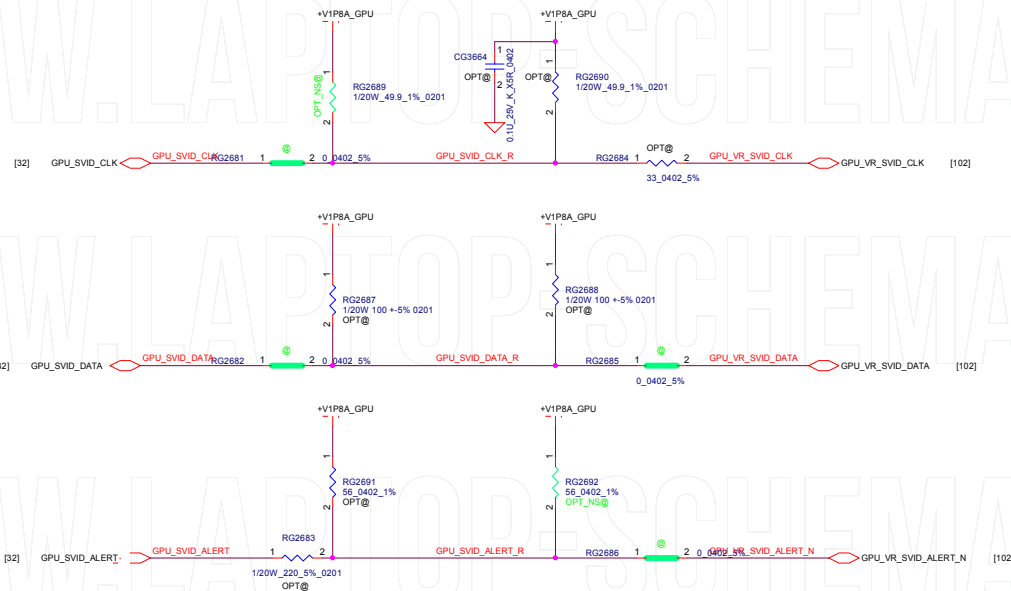


GDDR6_A_[63_32]



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GPU VREG: SVID



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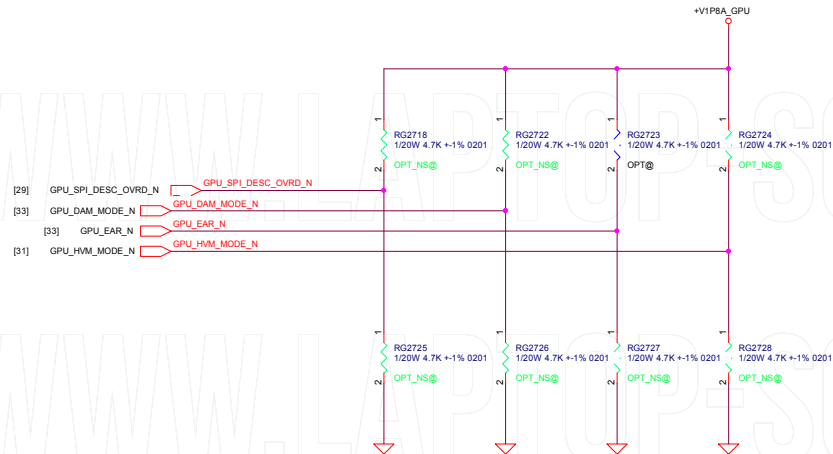
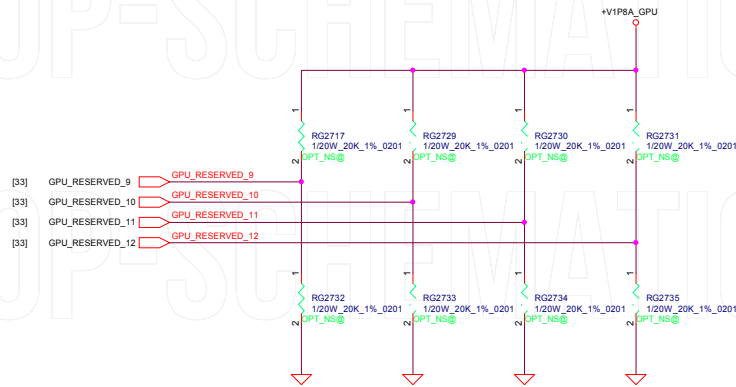
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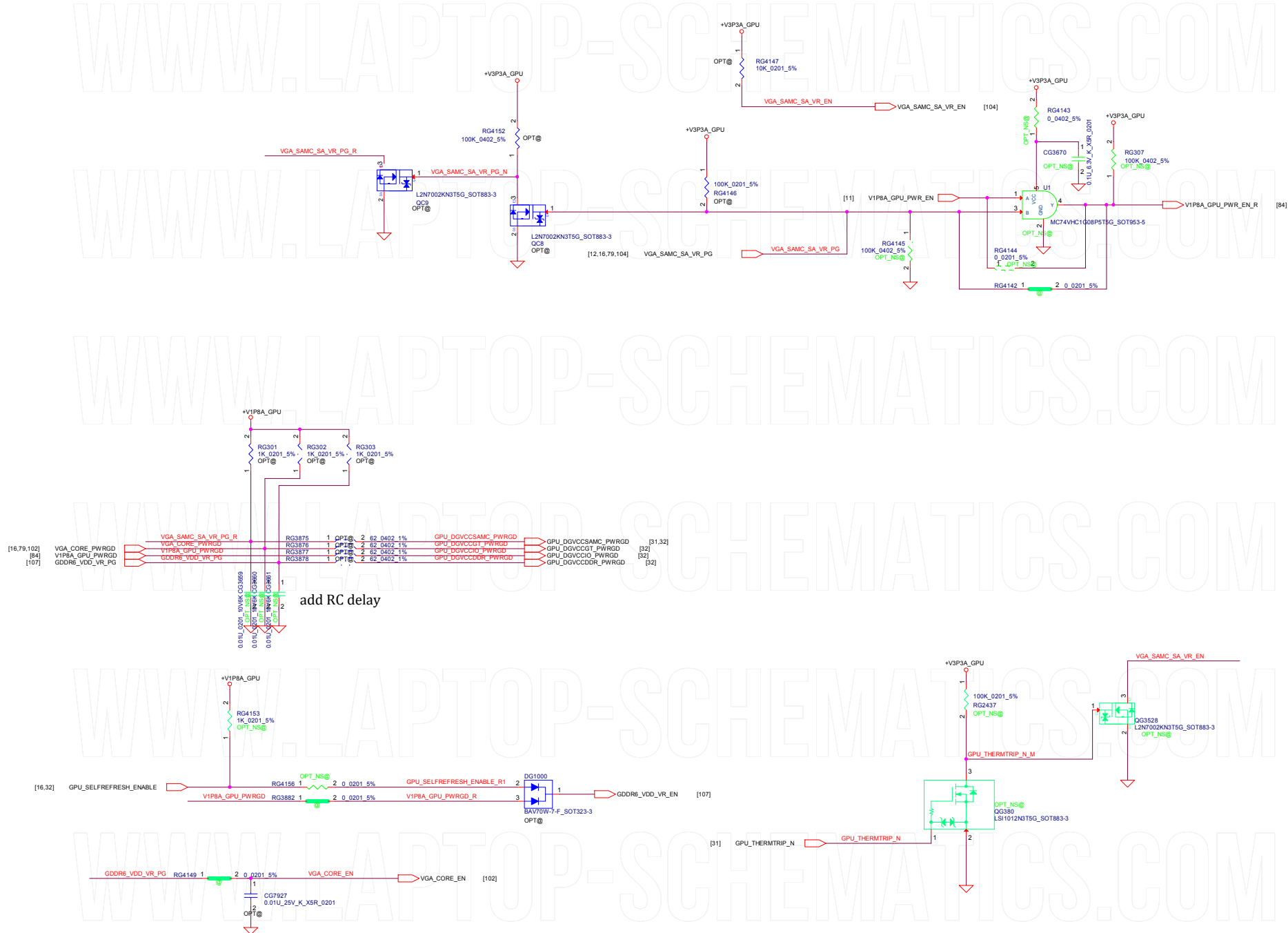
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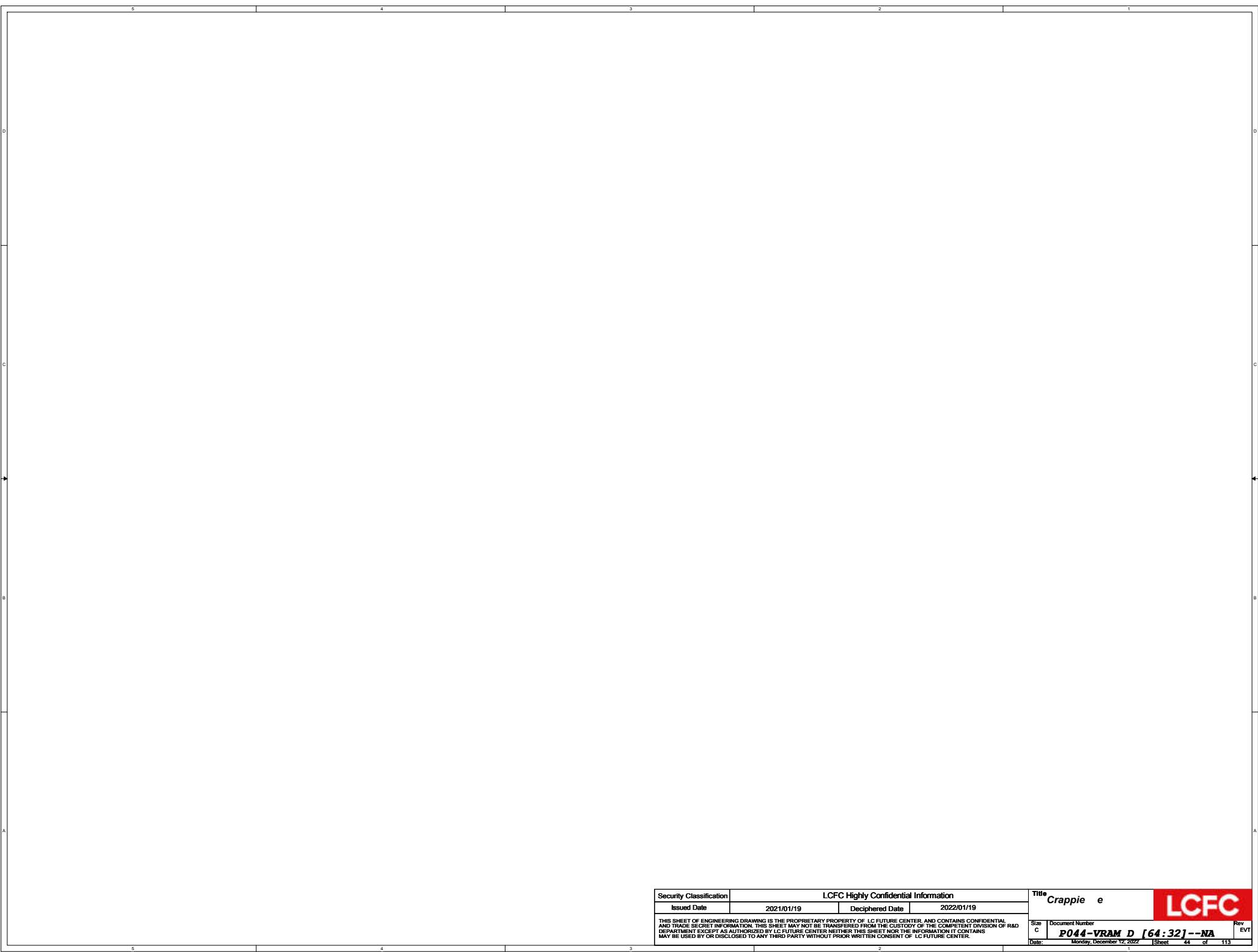
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GPU POWER SEQUENCING



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					C	P041-VRAM C [31:0]-NA		EVT
					Date	Narrative Description		Sheet
						1/2022		41 of 113



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Title		Crappie e		LCFC	
Size	Document Number	Rev		EVT	
C	P044-VRAM D [64:32]--NA				
Date	Monday, December 12, 2022	Sheet	44	of	113

5					4					3					2					1				
D																								
C																								
B																								
A																								

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Issued Date	2012/07/01		Deciphered Date	2014/07/01		Size B	Document Number			eDP MUX	Rev	0.1					
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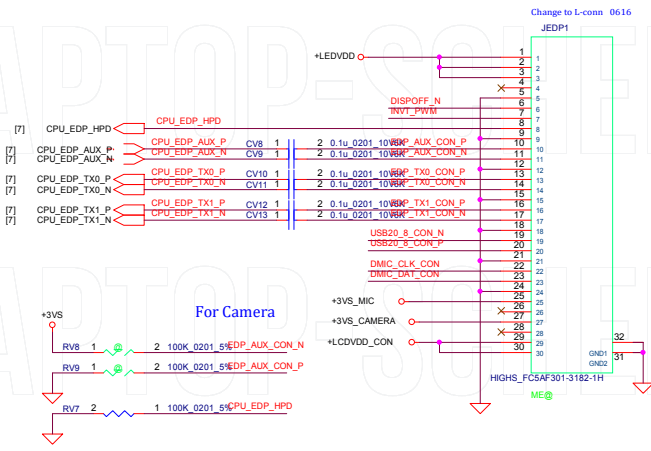
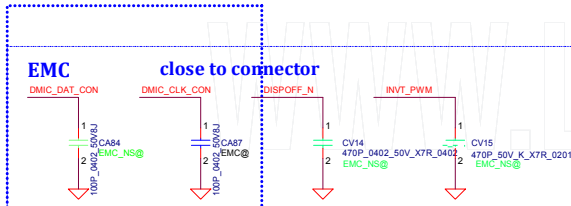
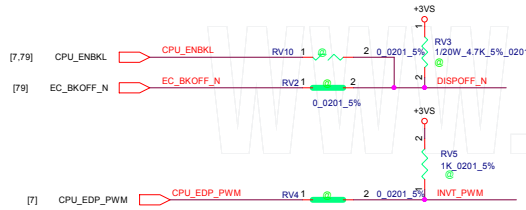
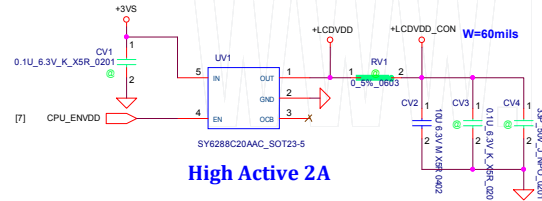
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Size	Document Number	eDP MUX			Rev
B					0.1
Date:	Monday, December 12, 2022			Sheet	45 of 110
		1			

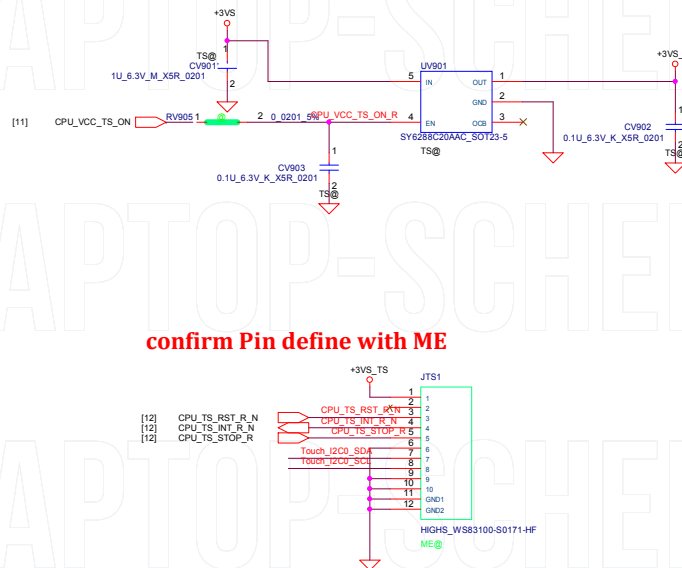
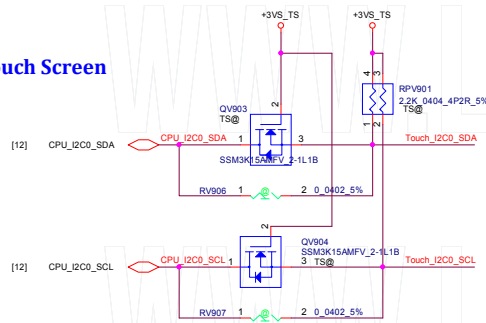
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				Date:	Monday, December 12, 2022	Sheet 46 of 110
		3			2	

LCD EDP Display

the diffrent with Base:
1.C970EDP connector pindefine different with S370&V14V15

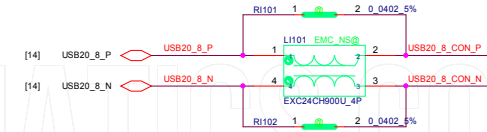
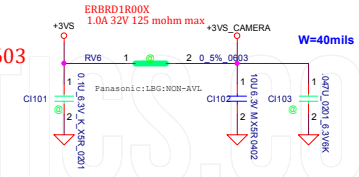


Touch Screen

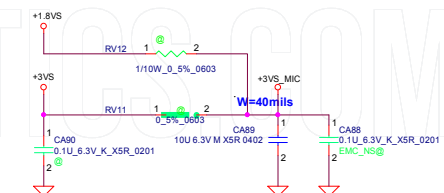


Camera

FI101 CHANGE TO 00HM 0603

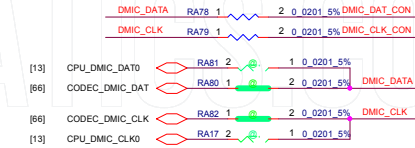


FA1 FA2 CHANGE TO 00HM 0603

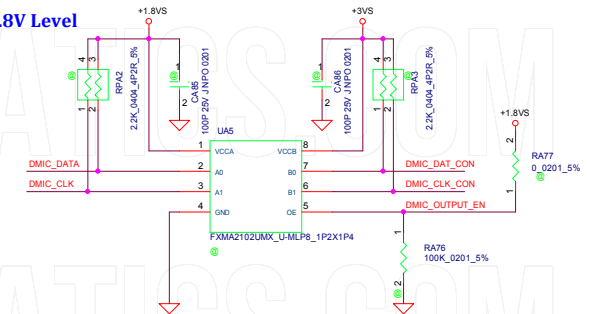



DMIC

DMIC 3.3V Level



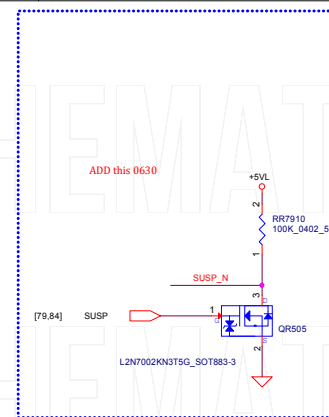
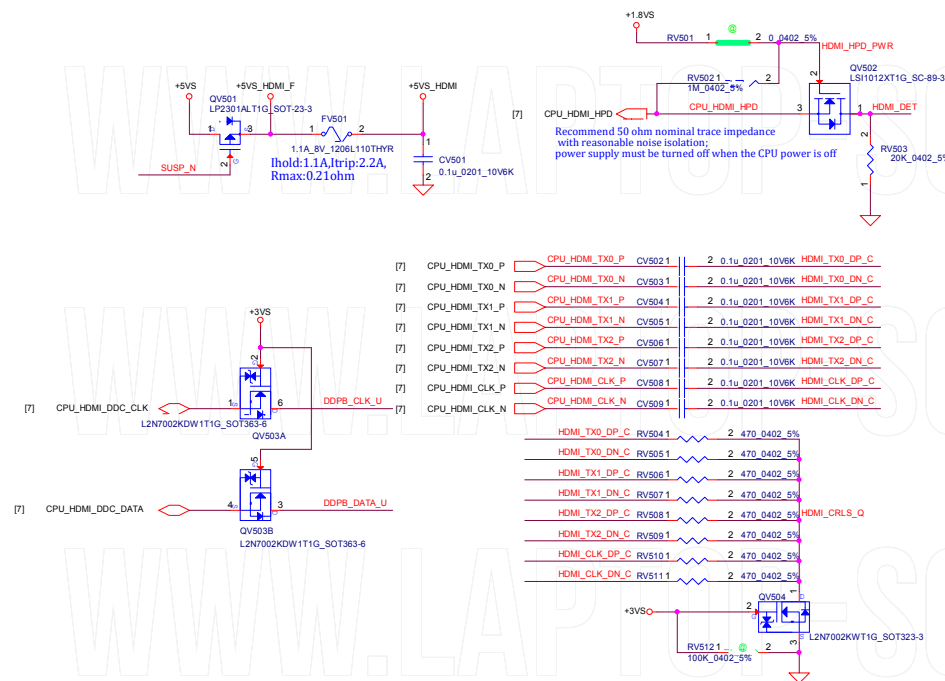
DMIC 1.8V Level



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				Sheet	48 of 110	Rev 0.1

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<table><tr><td>Security Classification</td><td colspan="3">LCFC Highly Confidential Information</td><td>Title</td><td colspan="2"><div>Crappie e</div><div>LCFC</div></td></tr><tr><td>Issued Date</td><td>2012/07/01</td><td>Deciphered Date</td><td>2014/07/01</td><td>Size B</td><td>Document Number</td><td>Rev</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td colspan="3">HDMI _ RETIMER0.1</td></tr><tr><td colspan="5">Date:</td><td>Monday, December 12, 2022</td><td>Sheet 49 of 110</td></tr></table>					Security Classification	LCFC Highly Confidential Information			Title	<div>Crappie e</div> <div>LCFC</div>		Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size B	Document Number	Rev	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				HDMI _ RETIMER0.1			Date:					Monday, December 12, 2022	Sheet 49 of 110
Security Classification	LCFC Highly Confidential Information			Title	<div>Crappie e</div> <div>LCFC</div>																											
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Date:					Monday, December 12, 2022	Sheet 49 of 110																										
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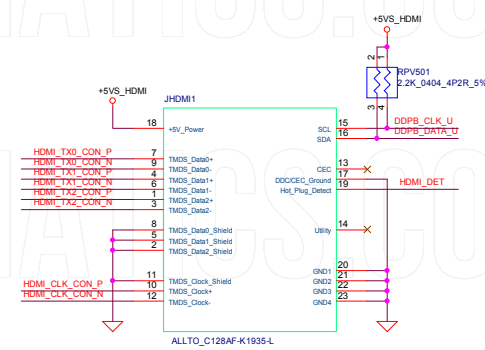
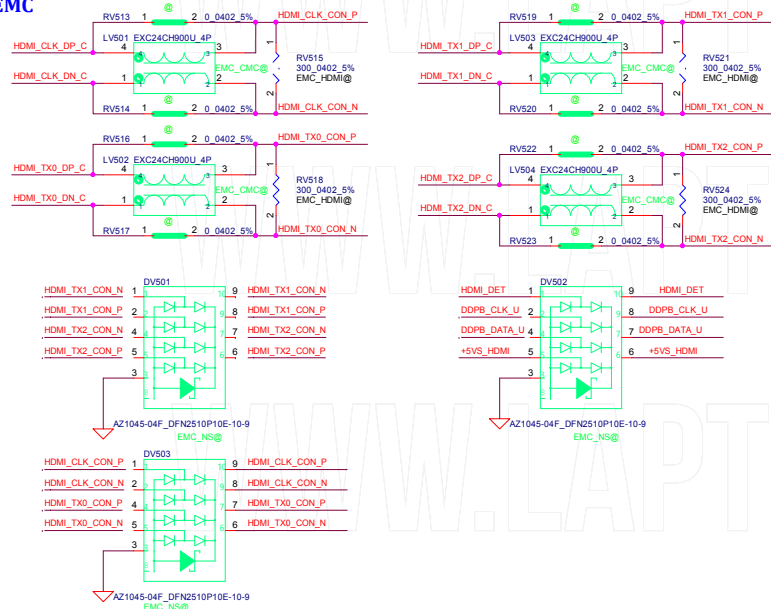
HDMI Power



the diffrent with Base:
1.C970 No HDMI CONN,S170 have

EMC

RV515 518 521 524 STUFF 300 FOLLOW S360?



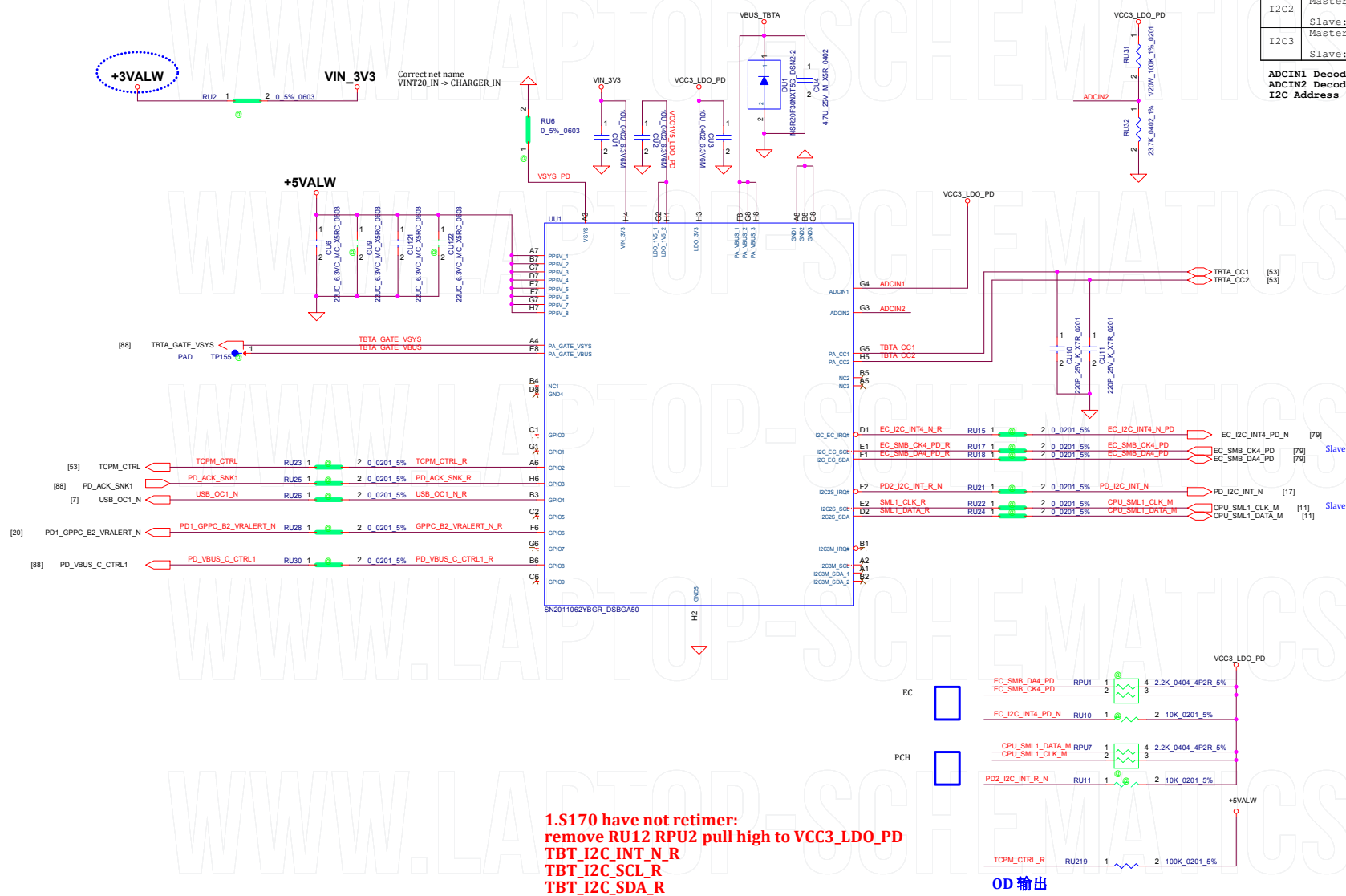
Conector list USE C128AF-K1939-L,Gold Plating diffrent

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Size	Document Number	HDMI_CONN			
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TABLE I2C Addressing

I2C1	Master: EC	TBTA PORT	0x20
	Slave: PD		
I2C2	Master: PMC	TBTA PORT	0x20
	Slave: PD		
I2C3	Master: PD	TBTA PORT	T.B.D.
	Slave: RT		

ADCIN1 Decoded: 7 --tie to LDO_3V3
 ADCIN2 Decoded: 4 --0.3022
 I2C Address Index: 1#





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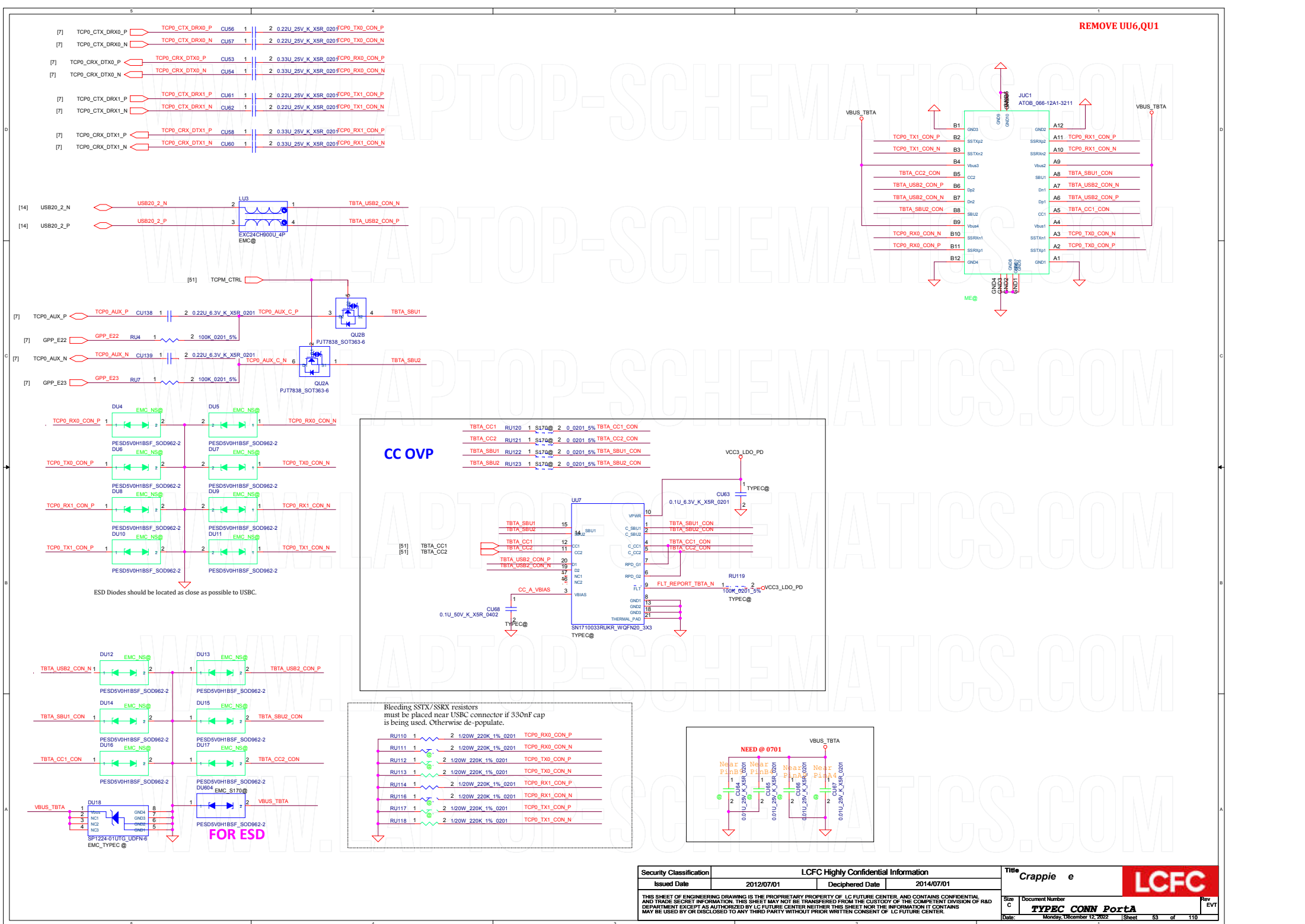
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Size C Document Number **TYPEC Controller Ports** Rev EVT
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						Rev 0.1
				Date: Monday, December 12, 2022		Sheet 52 of 110



REMOVE UU6,QU1

CC OVP

FOR ESD

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Size		Document Number				TYPE CONN Porta				Rev	
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										Date:		Monday, December 12, 2022		Sheet	54	of	110	

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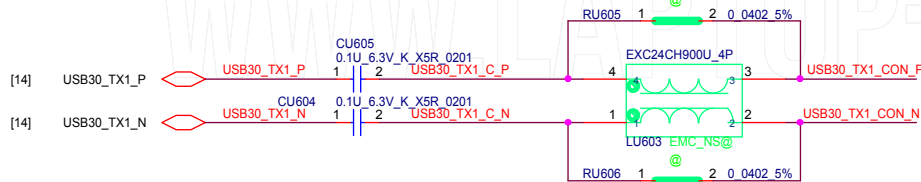
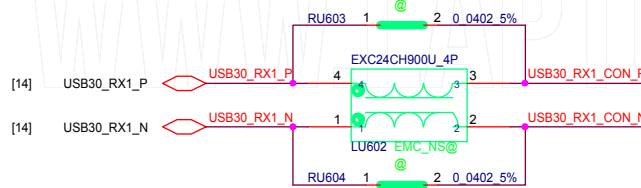
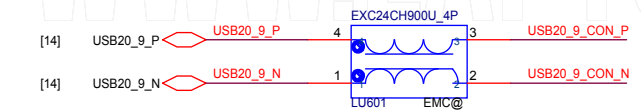
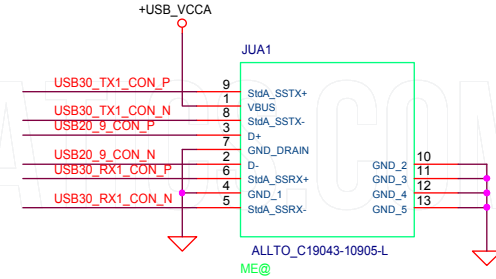
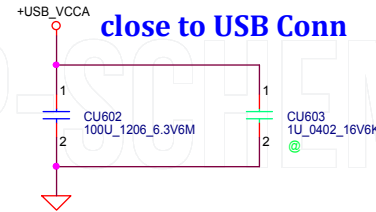
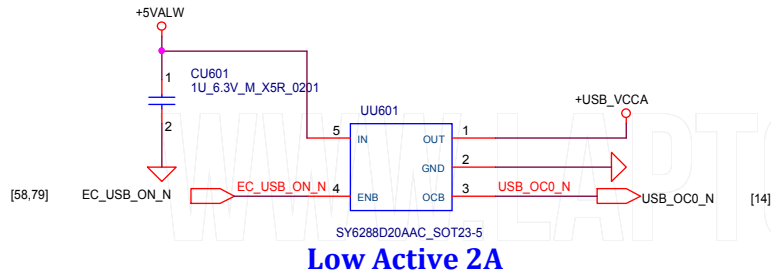
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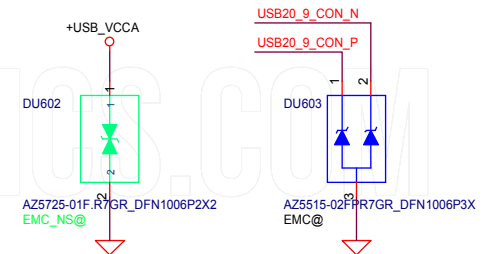
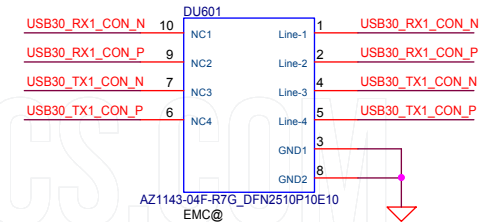
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Size	Document Number	TYPEC MUX PortB				Rev	0.1
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				Document Number	
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				Date:	Monday, December 12, 2022
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USB3.0 PORT



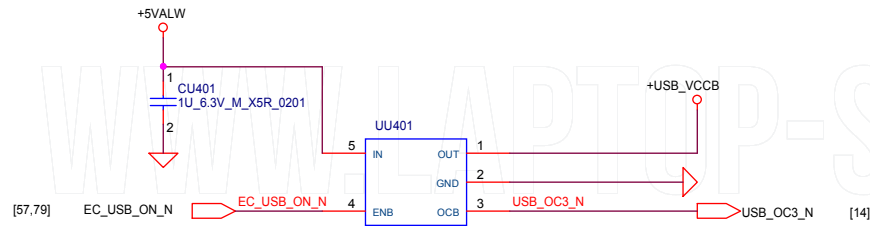
EMC close to USB Conn



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				USBA Porta		
				Date:	Monday, December 12, 2022	


USB2.0 Port and CMC&TVS&CAP MOVE to SUB Board


USB2.0 PORT



Low Active 2A


the diffrent with Base:
1.C970 No USB2.0 only,S360&V14V15 have

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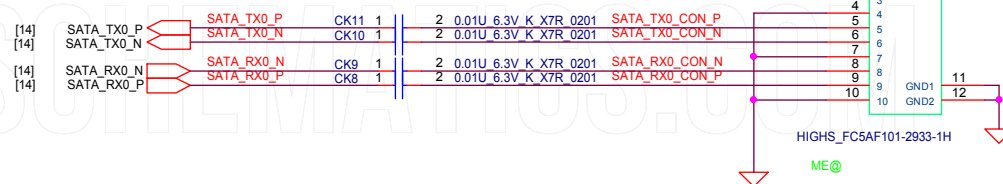
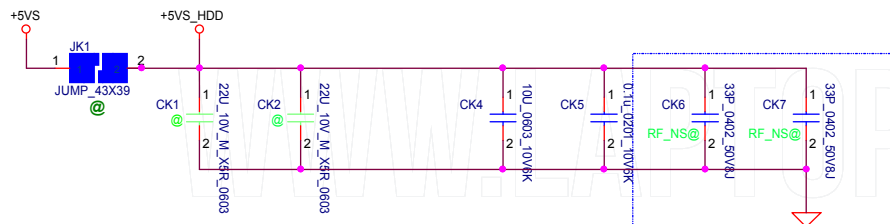
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								B	USB HUB					0.1
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HDD Power



Change to L-conn 6/17

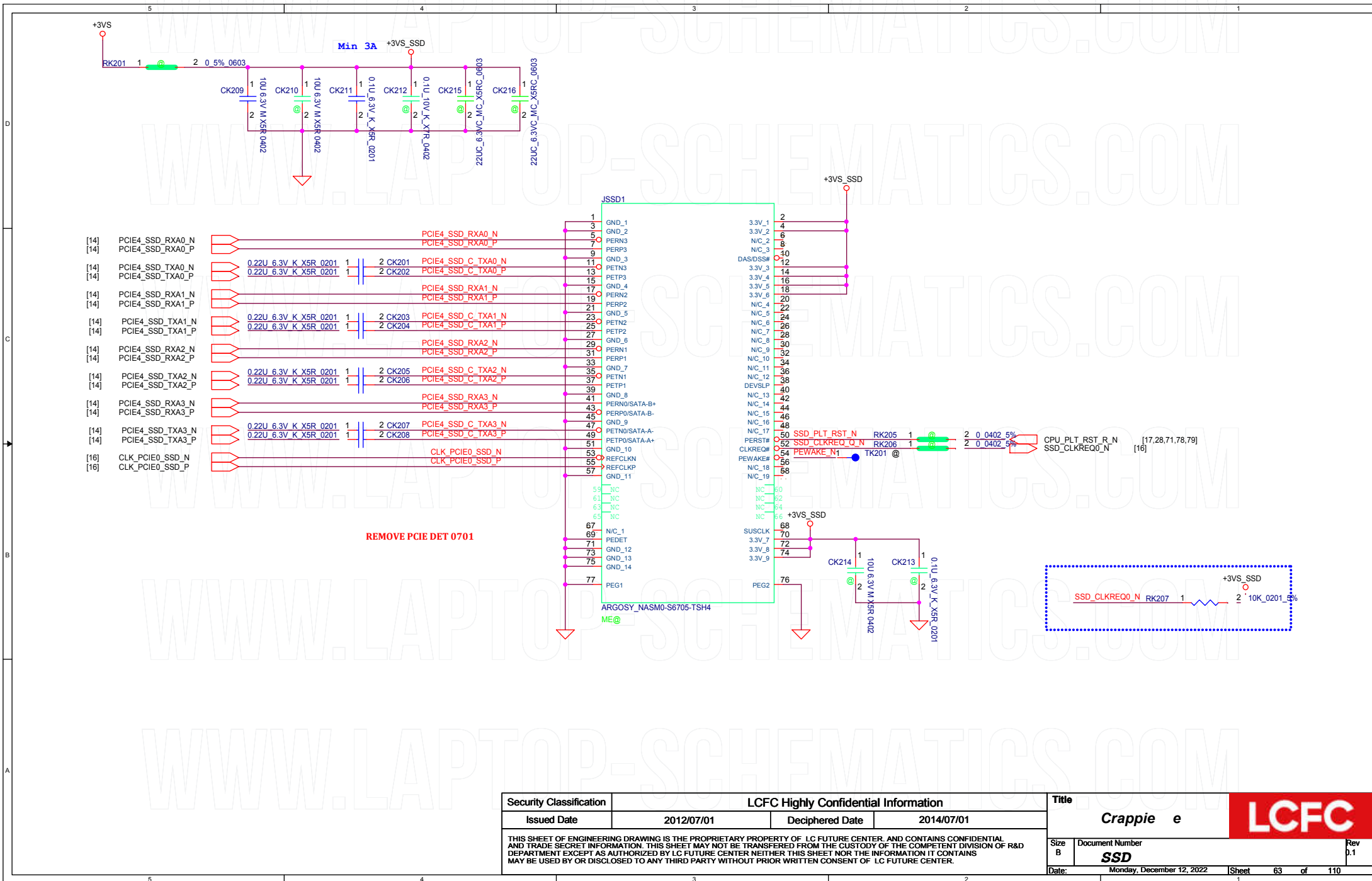
REXT: external res for output swing adjustment
it can be left open or tie to GND, internally generated bias
current can be used and the output is as default swing setting;

the pin can be connected 4.99k to GND, the output swing
will be at the default value with Reference to the ex RES


DEW: De-emphasis width setting for A&B

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Date:		Monday, December 12, 2022		Sheet	61	of	110	

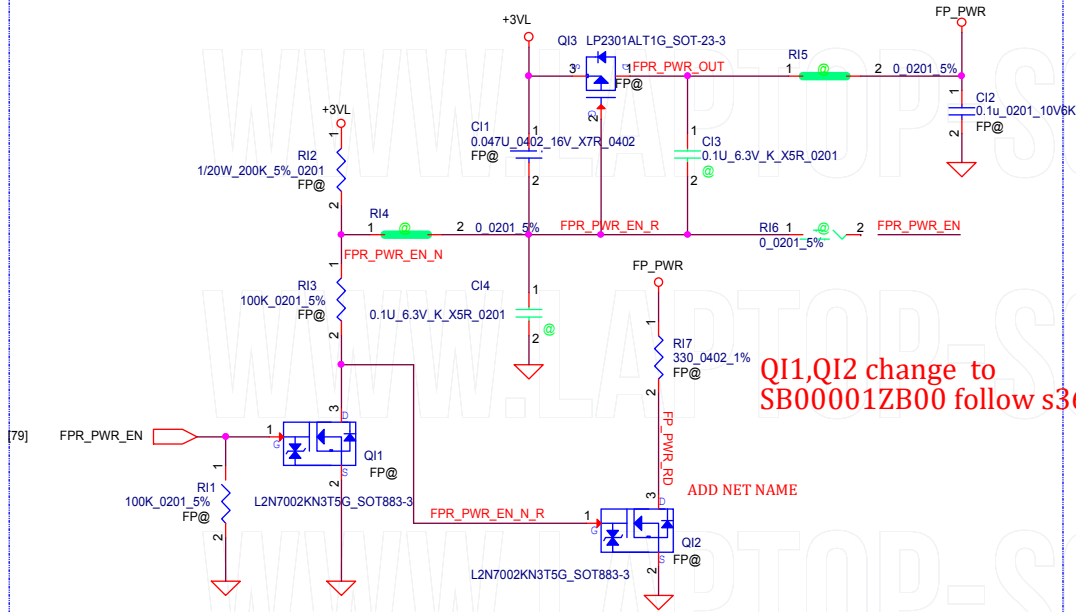
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	ODD			0.1
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Size B		Document Number				SSD		Rev 0.1	
Date:		Monday, December 12, 2022				Sheet 63 of 110			

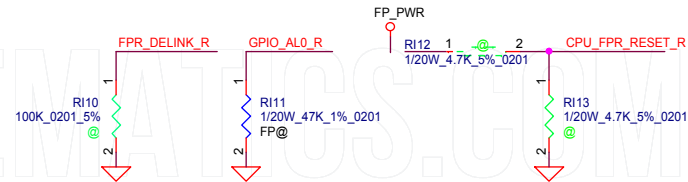
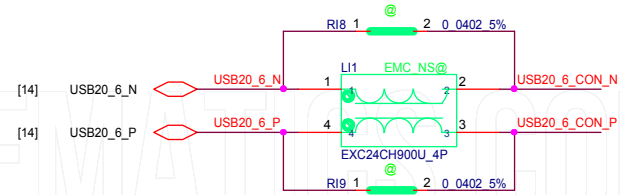
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		3	2		Date: Monday, December 12, 2022	Sheet 64 of 110

FP Power Control

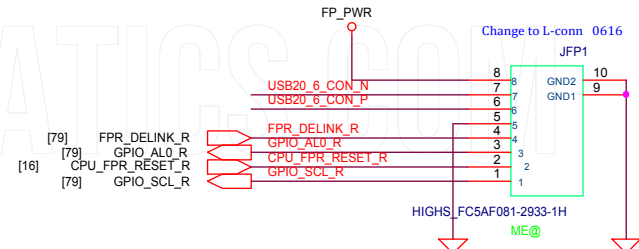
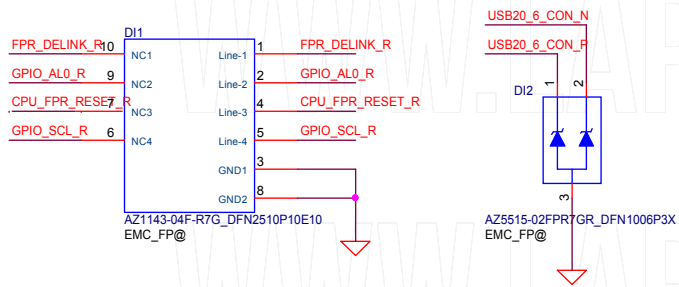


QI1,QI2 change to SB00001ZB00 follow s360

ADD NET NAME

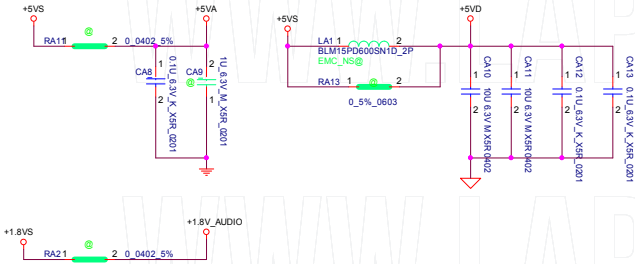
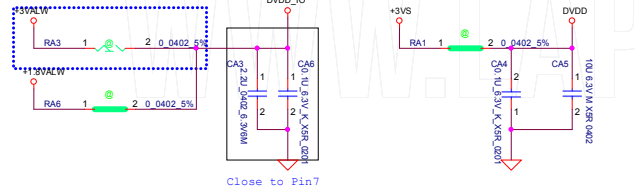


EMC close to Conn

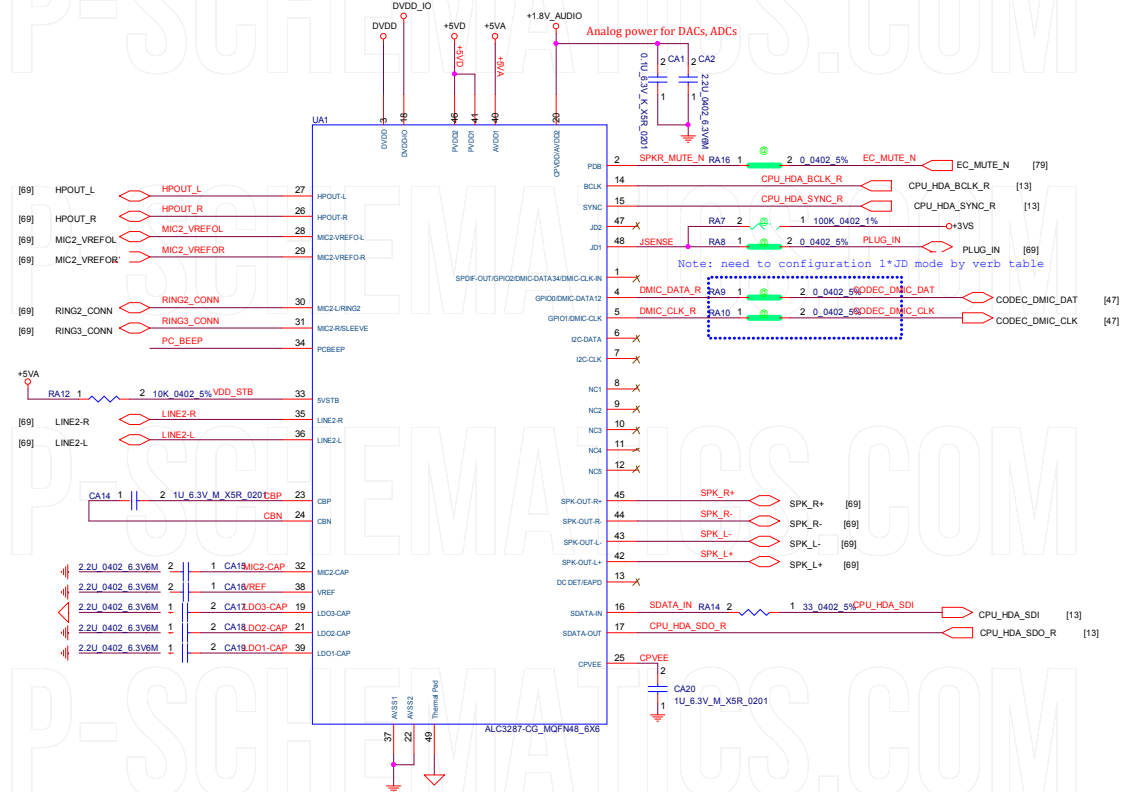


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Date:		Monday, December 12, 2022		Sheet		65		of 110	

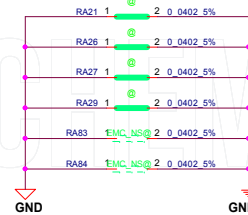
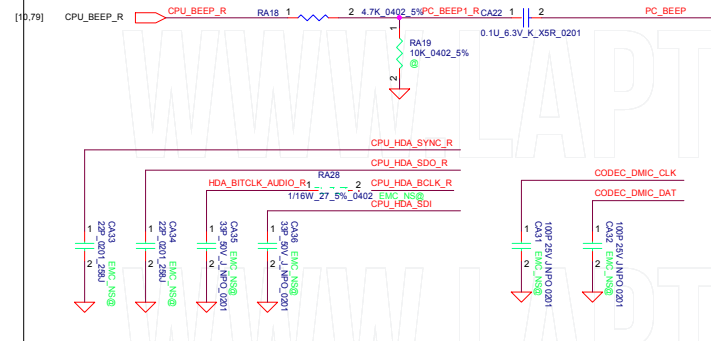
Note: DVDD-IO must be equal to or smaller than DVDD





- the different with Base MODULE:
- 1.Module no ra3 to DVDD_IO,S360&V14&V15 reserve
 - 2.Module no ra5 CA21 to EC_BEEP,S360&V14&V15 reserve
 - 3.RA9&RA10 BOMStructure different with module

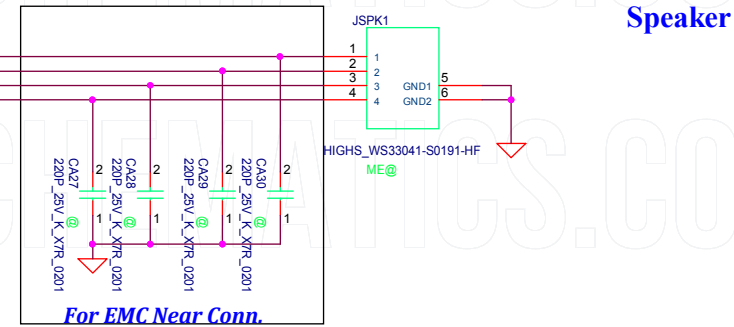
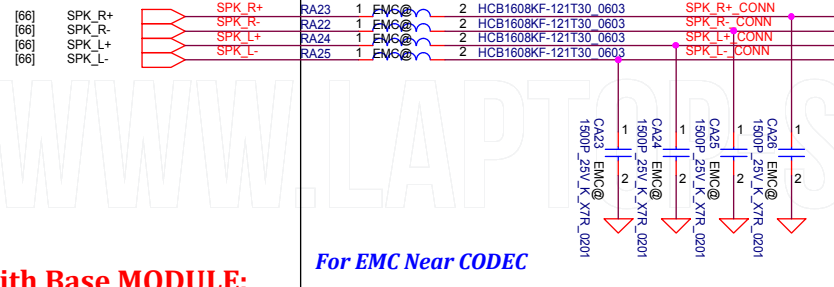


Note: power beep function is removed from BIOS spec



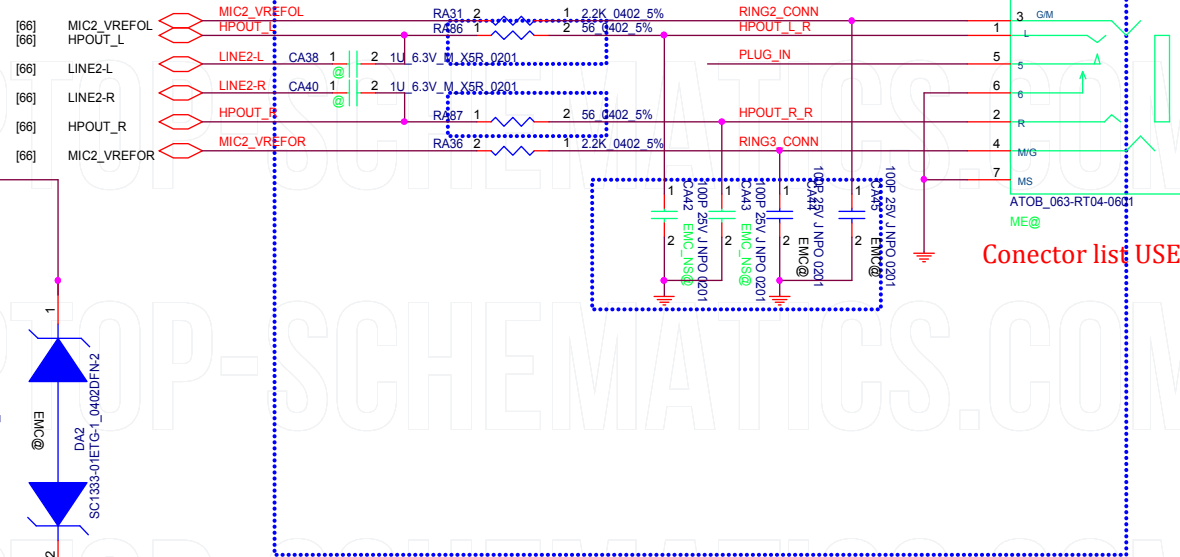
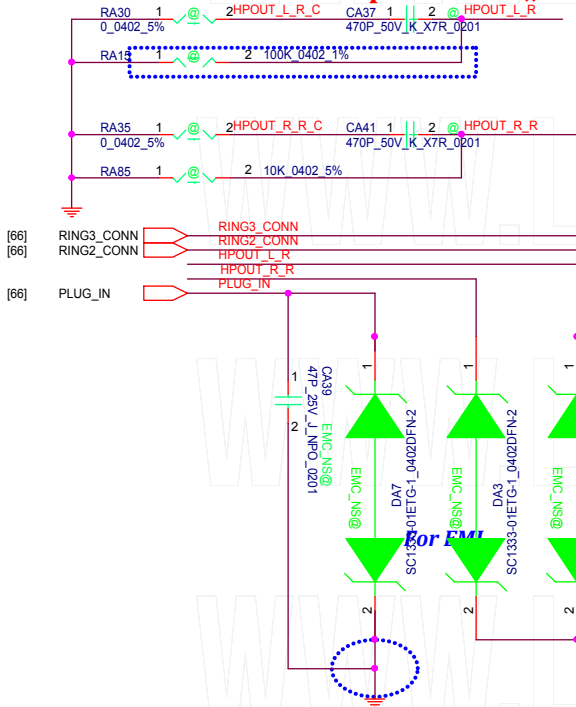
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				Audio Amplifier		
				Date:	Monday, December 12, 2022	Sheet 67 of 110

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				Date:	Monday, December 12, 2022	Sheet 68 of 110



the diffrent with Base MODULE:
 1.S360&V14&V15 RA86&RA87 VALUE different with module,
 Module have RA85&RA88,S360&V14&V15 Remove
 2.for EMC TVS EMC_NS@ type different with module
 3.GND type different
 4.module no CA37&CA41 part circuit,,S360&V14&V15 reserve

6pin&7pin audio jack comon design,stuff 6pin default;
 need vitrual symbol control




Conector list USE 063-RT04-0701

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Title		Crappie e	
Size B	Document Number	Audio SPK/Jack	
Date:	Monday, December 12, 2022	Sheet	69 of 110

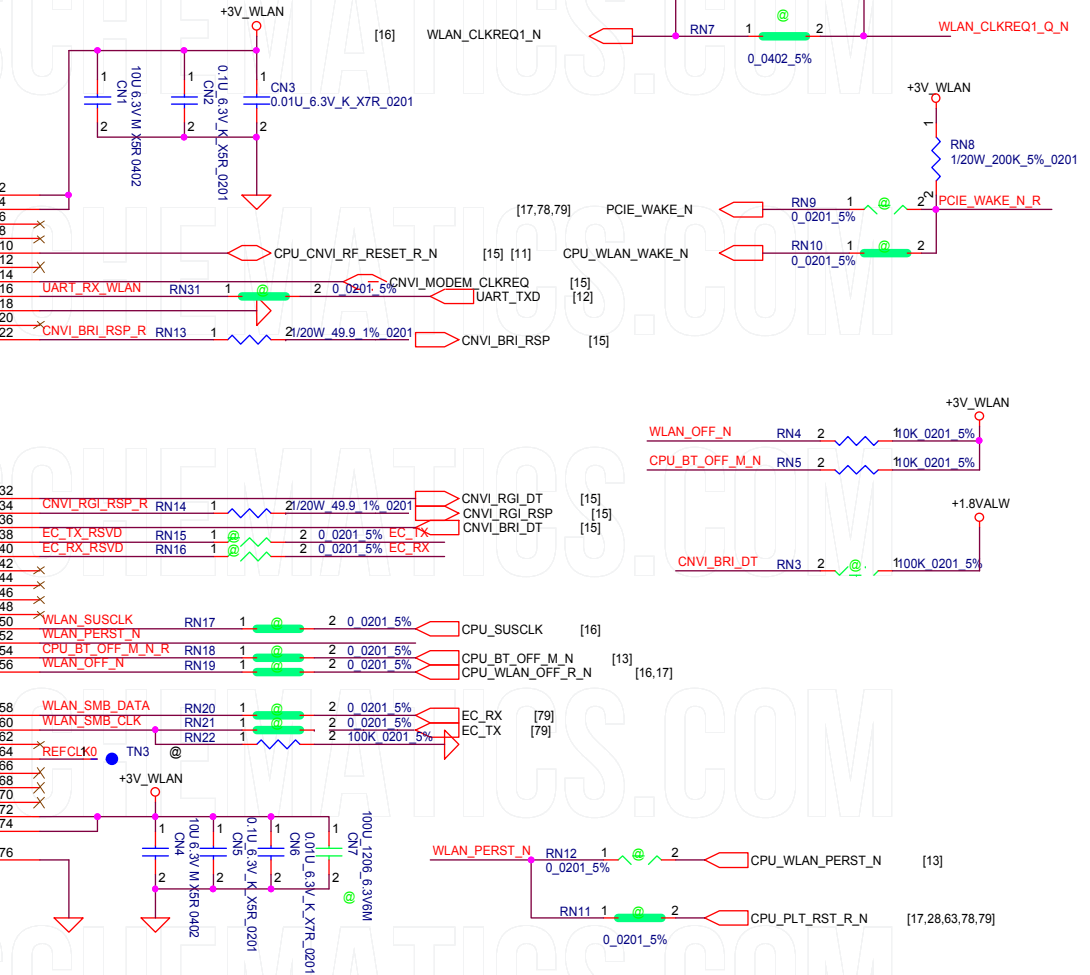
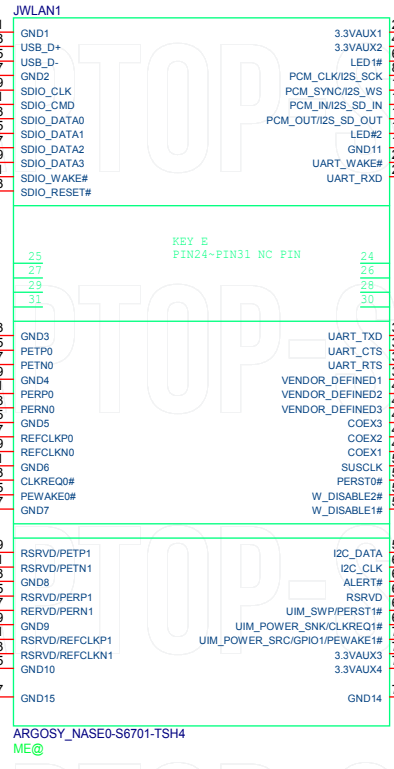
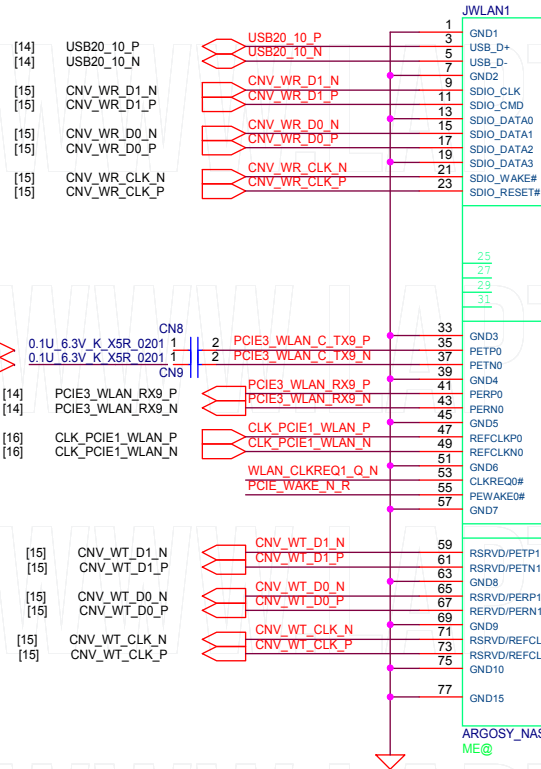
LCFC

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				Card Reader		
Date:				Monday, December 12, 2022	Sheet 70 of 110	



WLAN



Signal: CPU_BT_OFF_M_N
Voltage Level: 1.8V
LSI1012XTIG_SC-89-3
Vds max=20V
Vgs max=+/- 6V
Vgs(th)=0.45V/0.9V(min/max)
Rds(on)=1.25ohm(max,Vgs=1.8V)
Id=350mA(TA=25°C)
Ton Delay=5ns
Rise time=5ns



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Size B	Document Number		Rev		
	WLAN		0.1		
Date:		Monday, December 12, 2022		Sheet	71 of 110

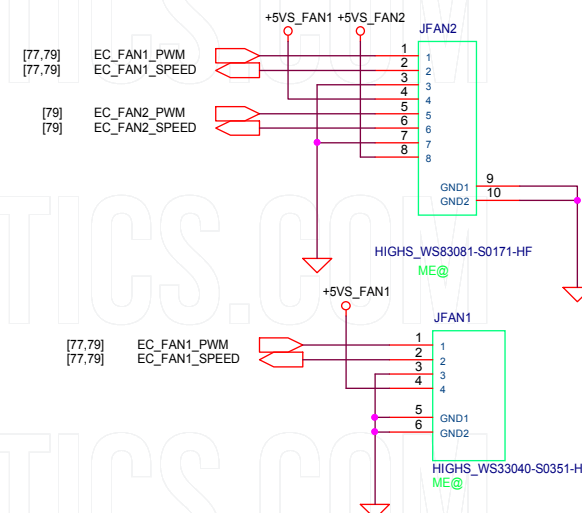
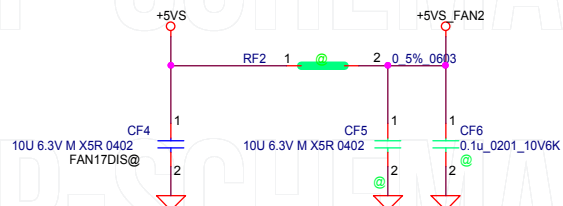
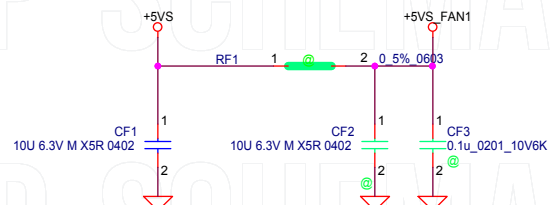
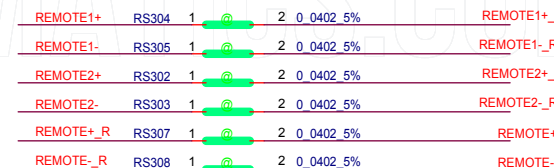
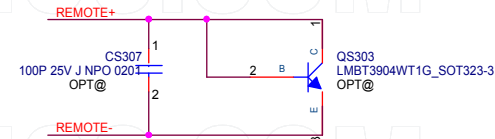
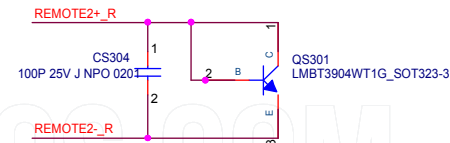
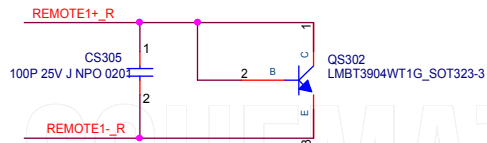
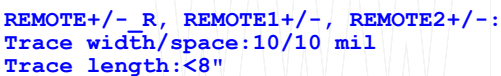
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				Date:		Monday, December 12, 2022		Sheet 73 of 110	

The figure is a large, empty rectangular area, likely a placeholder for a drawing or image. It is bounded by a thin black line. At the bottom right corner, there is a small table with the following content:

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				Sheet 75 of 110	

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				Date:	Monday, December 12, 2022	Sheet 76 of 110

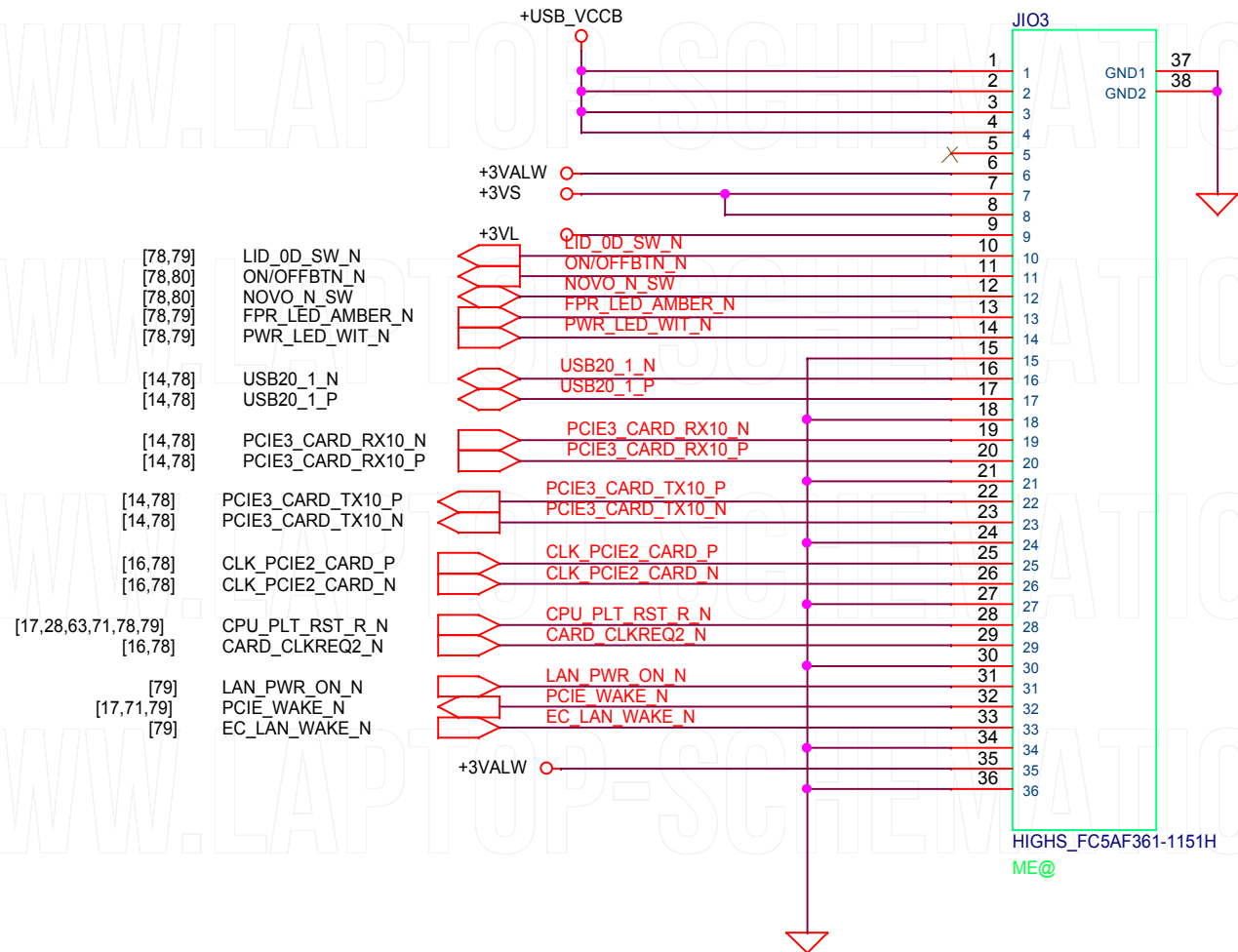


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				B	Thermal	0.1	
				Date:	Monday, December 12, 2022	Sheet	77 of 110


FPC+cable+Wire

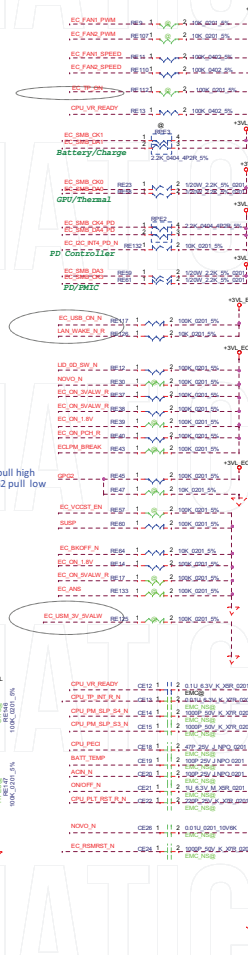
36PIN FOR LAN

Change to L-conn 0616



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Title			
Size B	Document Number	Rev	
	<i>Sub Board CONN</i>	0.1	
Date:	Monday, December 12, 2022	Sheet	78 of 110

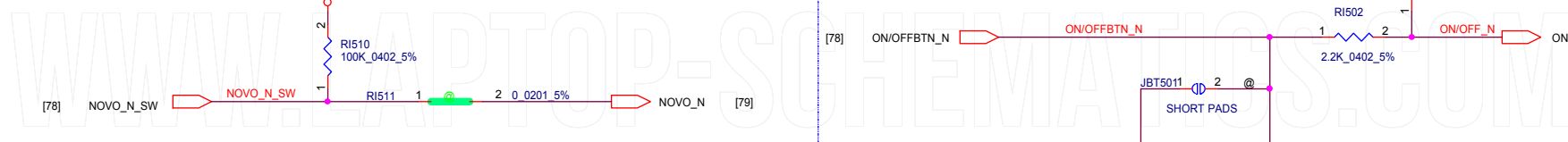


NOVO switch

[78] NOVO_N_SW \rightarrow NOVO_N_SW \rightarrow RI510 100K_0402_5% \rightarrow RI511 100K_0402_5% \rightarrow NOVO_N [79]

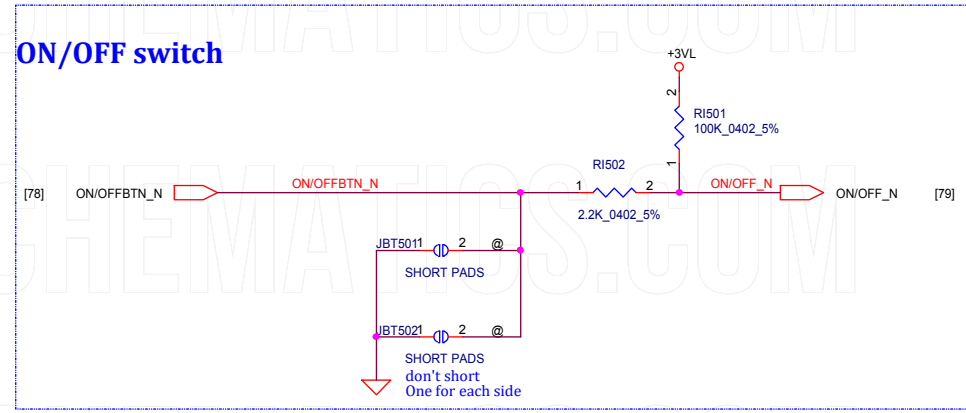
ON/OFF switch

[78] ON/OFFBTN_N \rightarrow ON/OFFBTN_N \rightarrow RI502 2.2K_0402_5% \rightarrow RI501 100K_0402_5% \rightarrow ON/OFF_N \rightarrow ON/OFF_N [79]

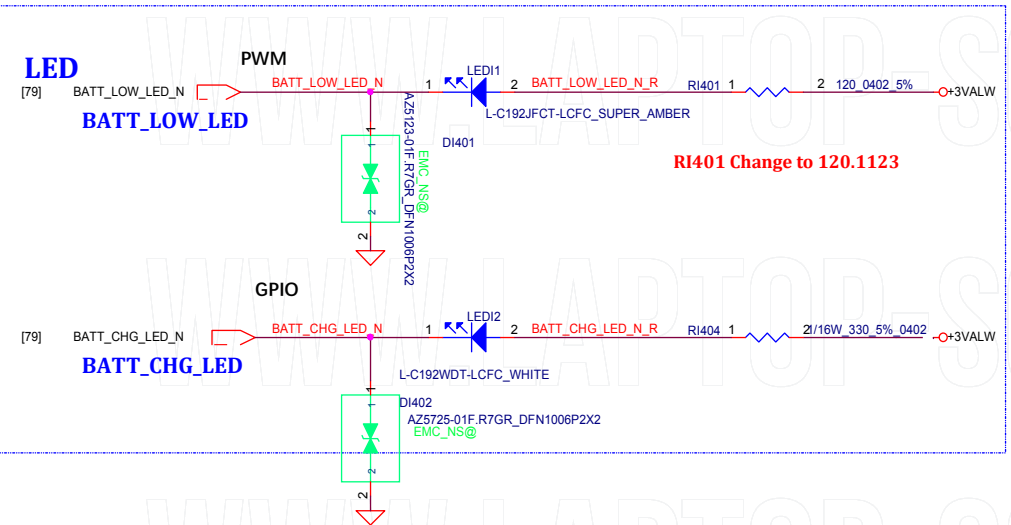


ON/OFF switch

The diagram shows a schematic for an ON/OFF switch. A +3VL supply is connected to a 100K resistor (RI501). The other end of RI501 is connected to a 2.2K resistor (RI502). The signal ON/OFFBTN_N is connected to the ON/OFF_N signal through a 2.2K resistor. The switch is implemented using two JBT5011 and JBT5021 transistors, with short pads indicated for each side.



the diffrent with module:
1.module1 mos control LED,S370&V14V15 NO NEED



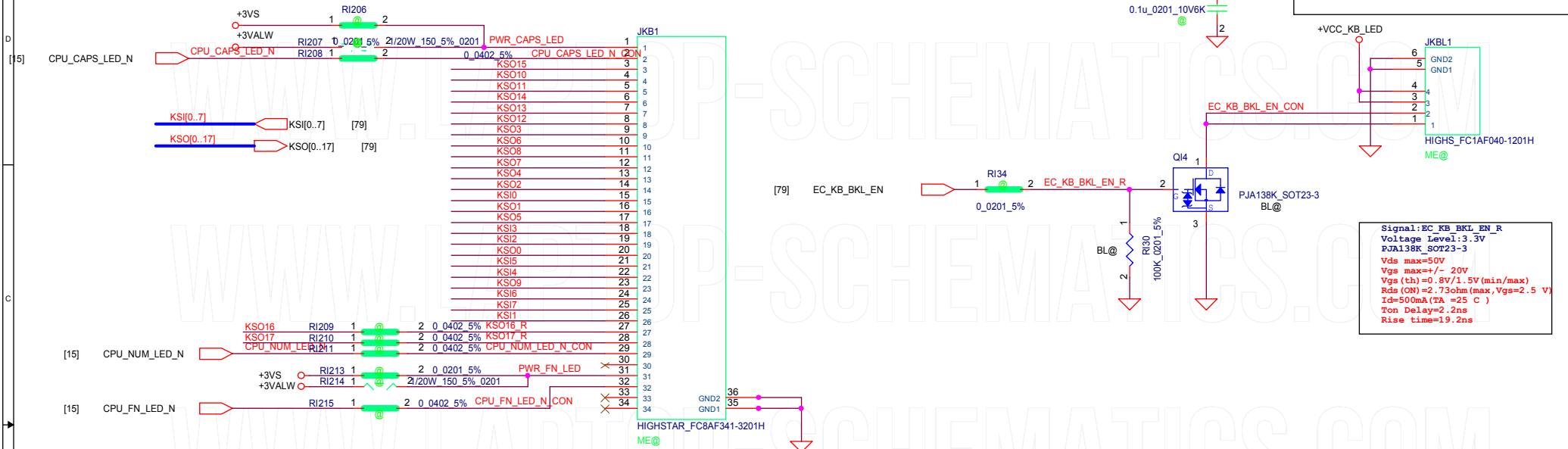
The Power LED move to SUB board LENS

LED	Stute	LED Behavior
Power Button	System on	White_on (battery: 21%-100%)
		Amber_on (battery: 0%-20%)
	Standby LID closed	White_on (battery: 21%-100%)
		Amber_Blink_3S (battery: 0%-20%)
	System off	OFF
Charging	Battery only	OFF
	Charging	Amber_on (battery: 1%-90%)
		White_on (battery: 91%-100%)

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Title		Crappie e		LCFC	
Size B	Document Number LED/Button				Rev 0.1
Date:	Monday, December 12, 2022		Sheet	80	of 110

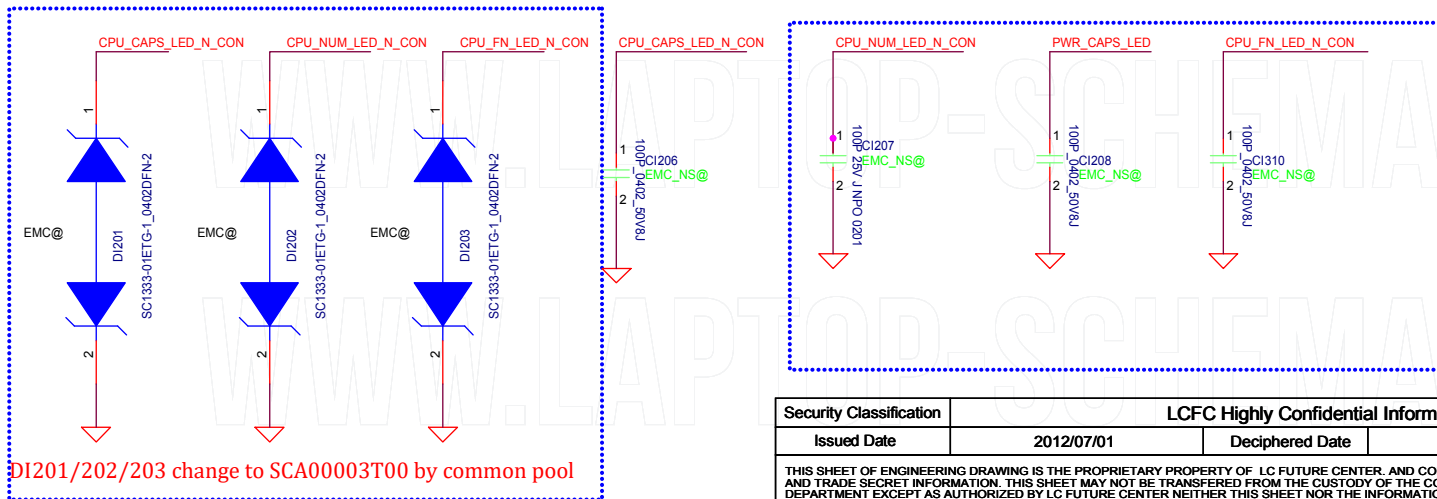
K/B Connector



BL CONN NEED CONFIRM WITH KEY BOARD SOURCE


Signal: EC_KB_BKL_EN_R
Voltage Level: 3.3V
PJA138K_SOT23-3
Vds max=50V
Vgs max=+- 20V
Vgs(th)=0.8V/1.5V(min/max)
Rds(on)=2.73ohm(max, Vgs=2.5 V)
Id=500mA(TA=25 C)
Ton Delay=2.2ns
Rise time=19.2ns

EMC close to Conn



D1201/202/203 change to SCA00003T00 by common pool

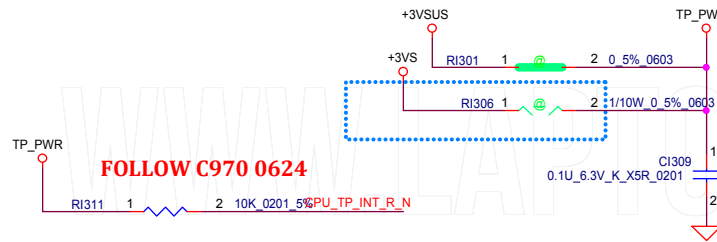
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Size B		Document Number								Rev 0.1
		KB/KBBL_CONN								
Date:		Monday, December 12, 2022						Sheet	81	of 110

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				Date:	Monday, December 12, 2022	Sheet 82 of 110

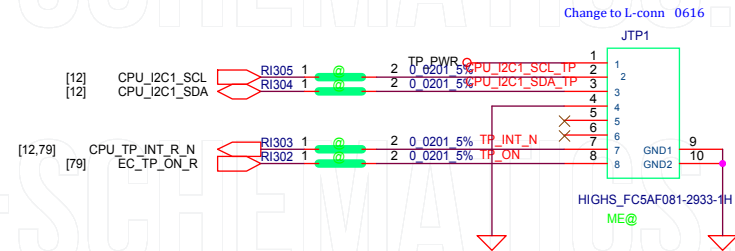
the diffrent with Base MODULE:
1.Module no RI306,S360&V14&V15 Rerserve

Touch Pad

Need support wake up by touch pad
 Follow latest UE spec



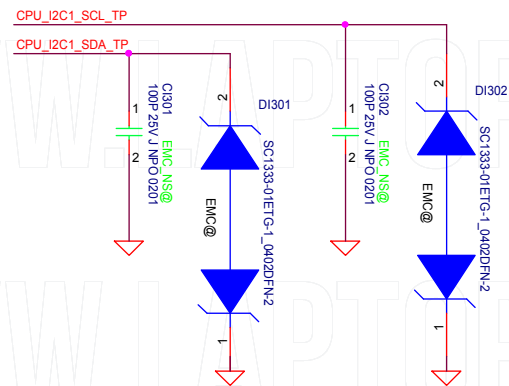
FOLLOW C970 0624



Change to L-conn 0616

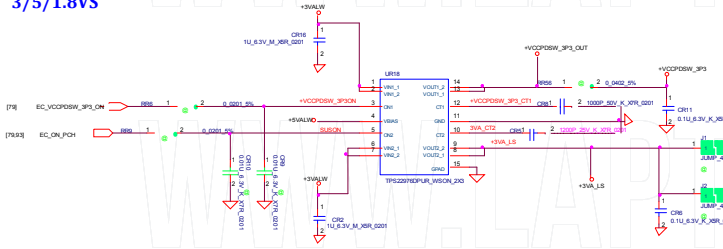
JTP1

HIGHS_FC5AF081-2933-1H
 ME@



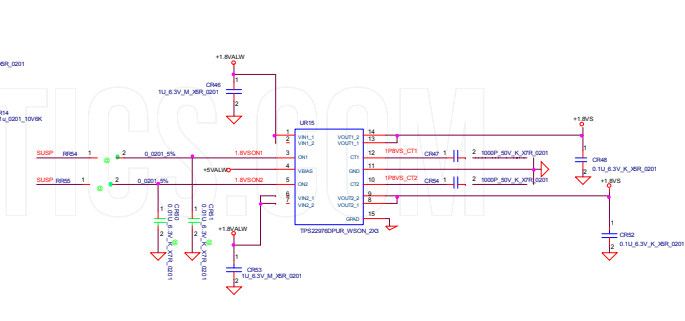
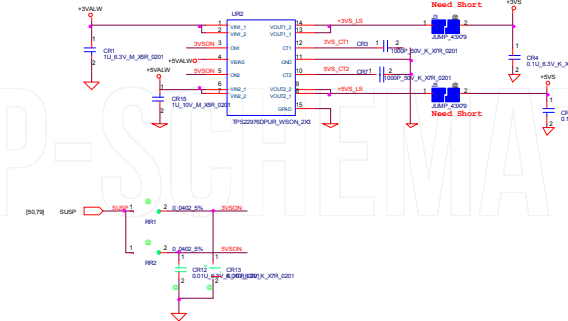
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Issued Date		2012/07/01		Deciphered Date		2014/07/01			
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B		TouchPad CONN						Rev 0.1	

3/5/1.8VS



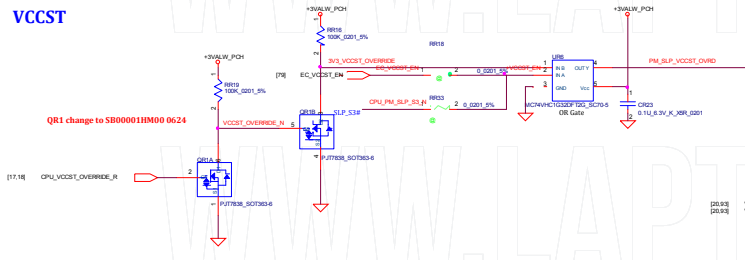
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 -> 2.74ms
+5VS, C176 -> 2.03ms
VIN 5V and 3.3V (VIAS=5V), MAX(per channel)=6A, Rd=16mohm

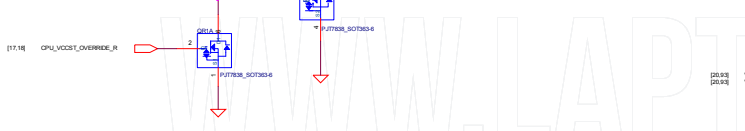


VCCST

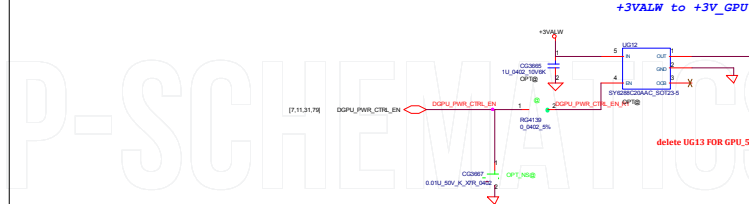
VCCST EN Signal modify 0624



QR1 change to SB000001HM00 0624



GPU POWER SWITCH

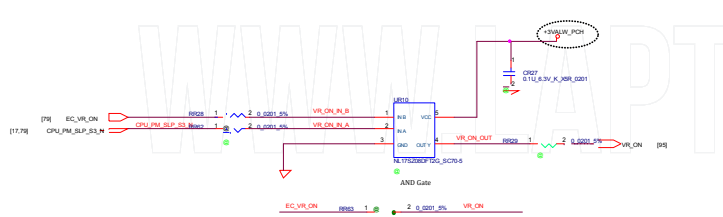


+3VALW to +3V_GPU

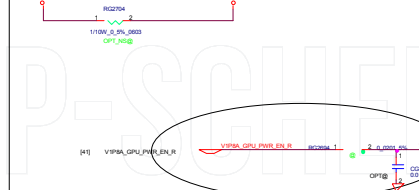


delete UG13 FOR GPU_VA 0716

VR_ON

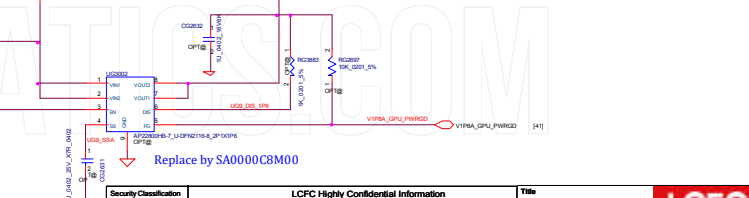


+1.8VALW



FOLLOW 630275
NEED TO FINE TUNE THE DELAY RESISTOR
WTR RAMPUP TIME OF +VCCSA GPU RAIL,
SUCH THAT +V 1P80A GPU COMES AFTER
+VCCSA GPU RAIL.

+1.8VALW

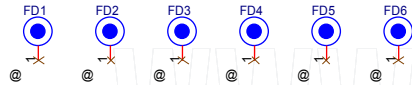


Replace by SA0000C8M00

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Date		Monday, December 12, 2011		81 d 110	

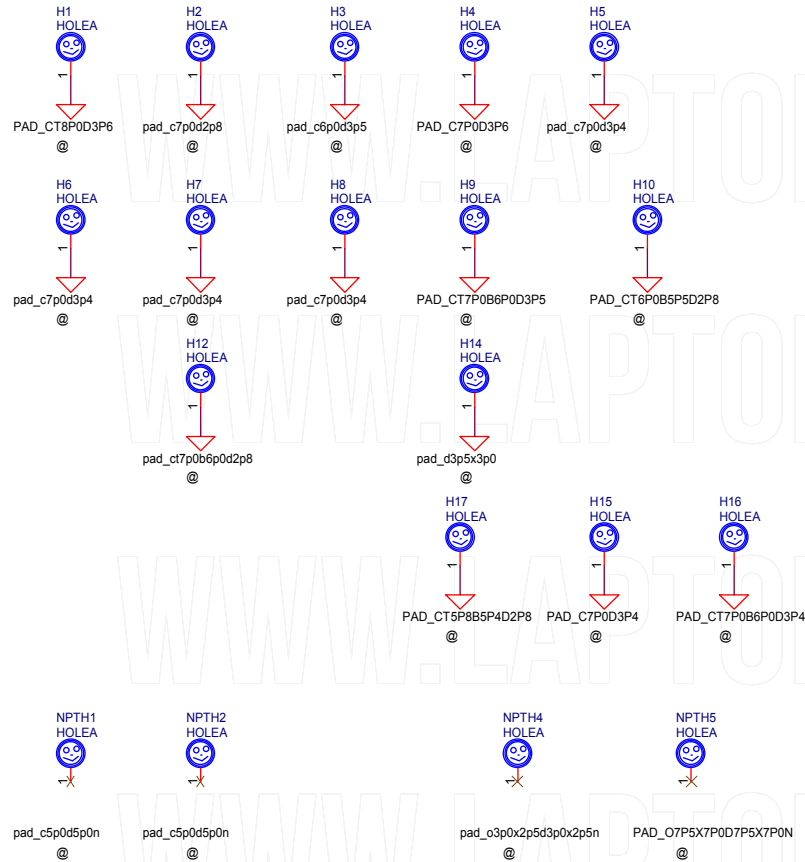
Security Classification		LCFC Highly Confidential Information		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	<div>Crappie e</div> <div>LCFC</div>	
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				Date:	Monday, December 12, 2022 Sheet 85 of 110

PCB Federal Mark PAD

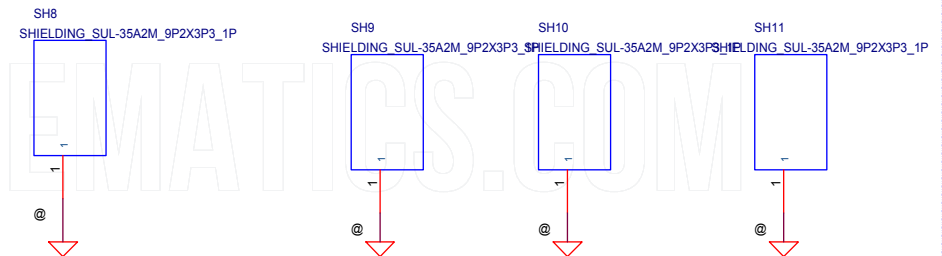


MD Shielding

Hole

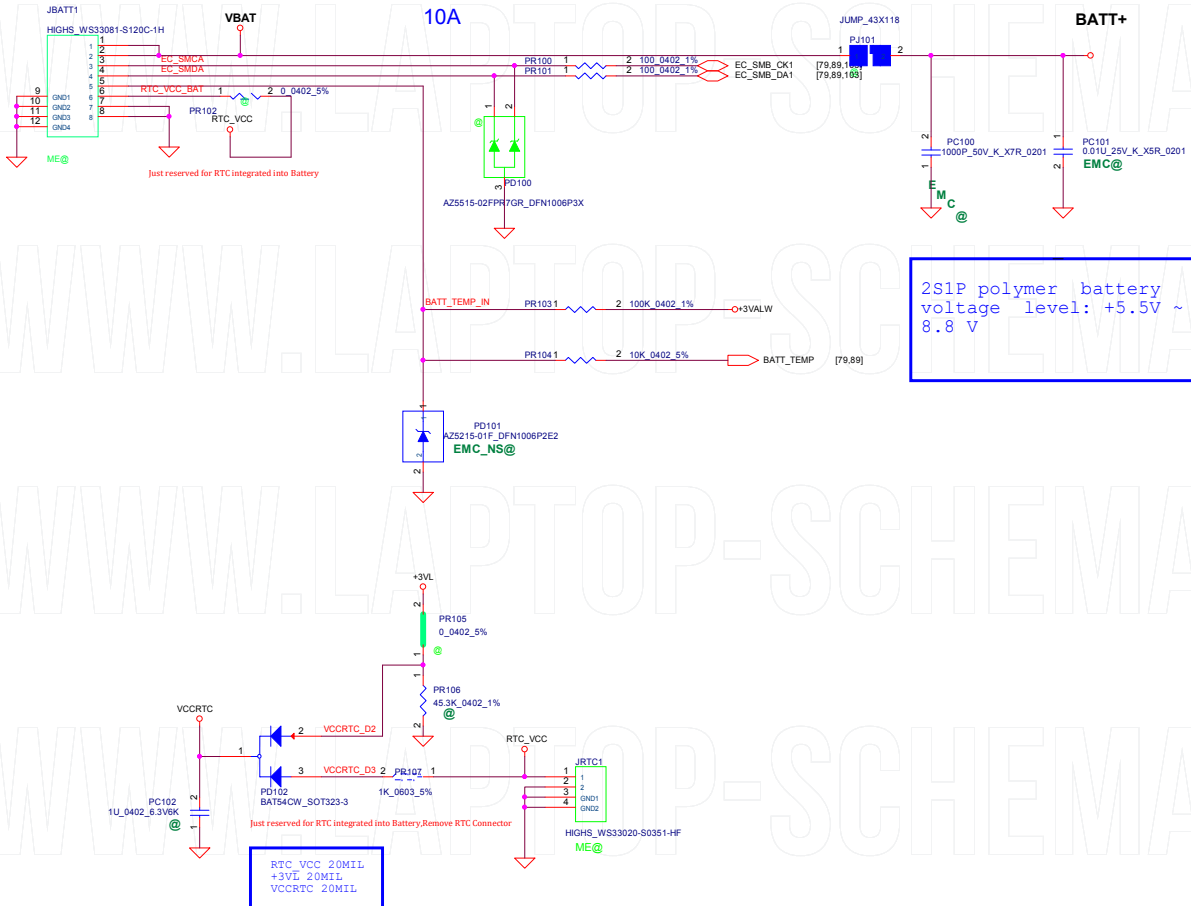


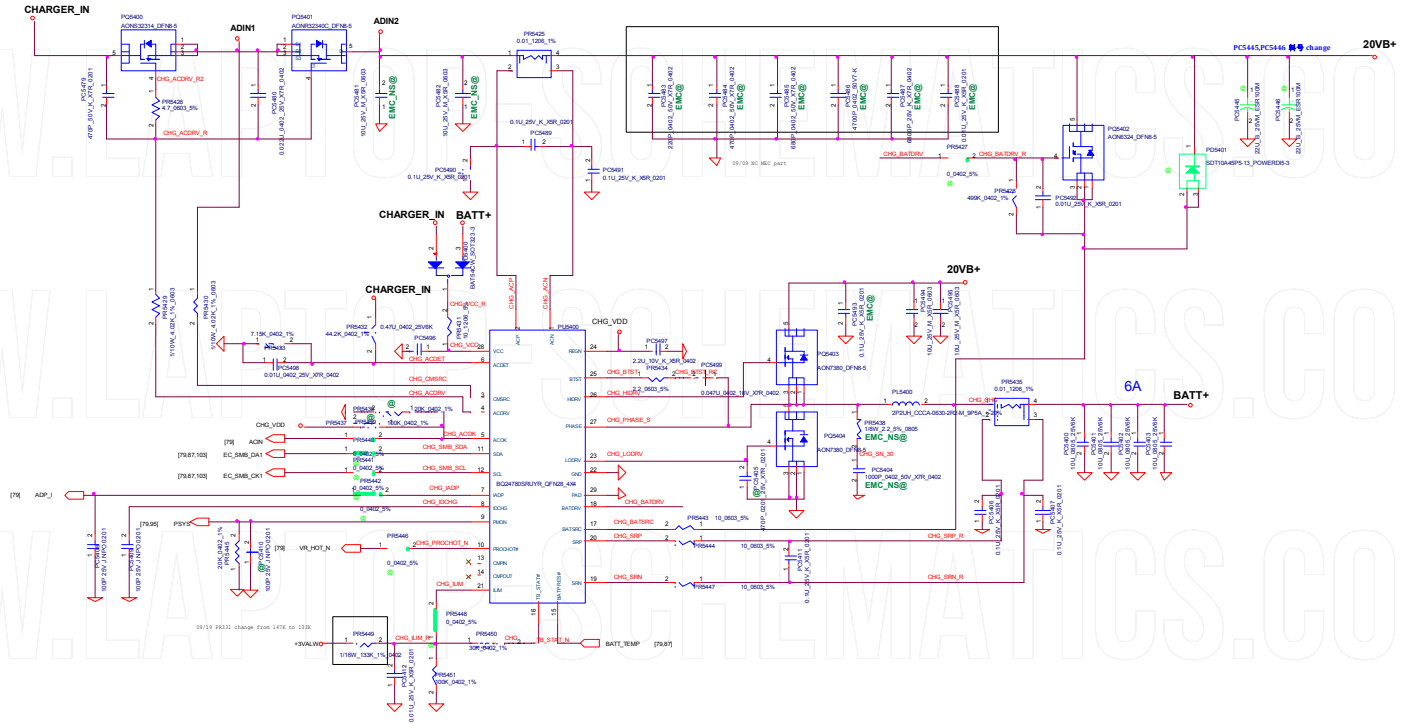
SO-DIMM Shielding



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Hole/Shielding		Rev	0.1
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ACDECT setting 17.2V
 Charge current limit HW=7A
 DC discharge limit =26A
 Discharge current limit HW=9A during Turbo boost

IDPM	V(ILIM)	PR5320
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K
4.0A	2.6V	162K

← LOGIC

VILIM=1V+40x (VACP-VACH)=1+40xIDPMxRAC

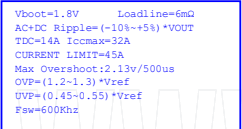
IND IN USE	PR5333
1uH	93K
2.2uH	137K
3.3uH	169K

← LOGIC

# of CELL	VCELL_PRES	PR5322
1-CELL	1.5V	301K
2-CELL	2.4V	150K
3-CELL	3.3V	82K
4-CELL	4.5V	33.2K

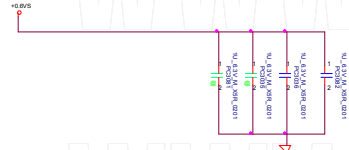
← LOGIC

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Issued Date	2021/01/19	Deciphered Date	2022/01/19	Crappie e		
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				Date: Monday, December 12, 2022	Sheet 90	of 110

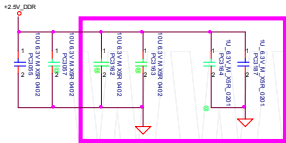


CHANNELA SLOT DIMM decoupling

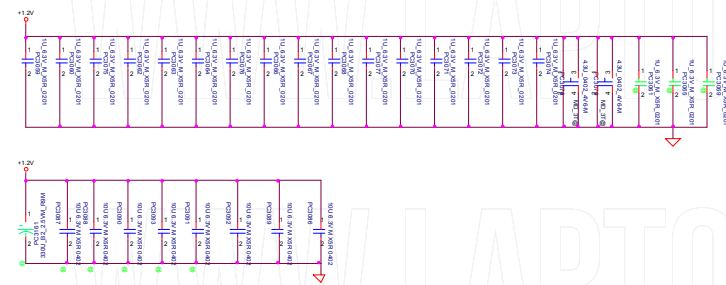
VTT
PDG 2 Channel SODIMM: 2*10UF(0603,1 placeholder)+4*1UF(0402)
S360: channel A:1*10UF(0402)+ 2*1UF(0201)



VPP
PDG 2 Channel SODIMM: 2*10UF(0603)+2*1UF(0402)
S360: channel A:1*10UF(0402)+ 1*1UF(0201)

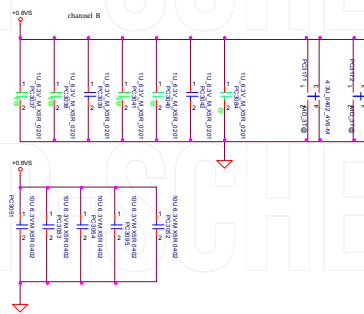


VDDQ
PDG 2 Channel SODIMM: 1*330UF(7343)+16*10UF(0603)+16*1UF(0402)
S360: channel A:8*10UF(0402)+ 16*1UF(0201)

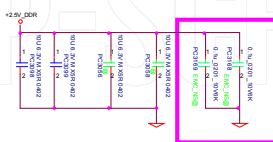


CHANNELB MD decoupling

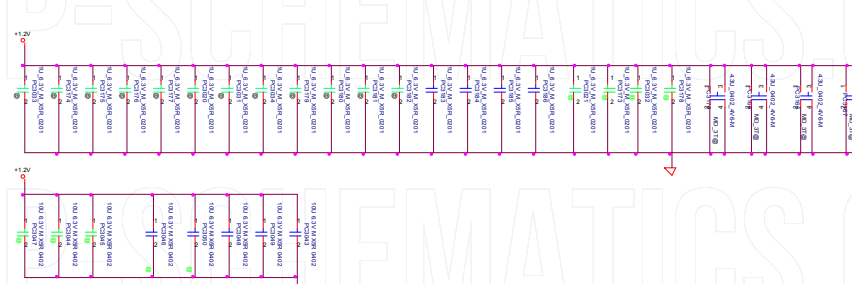
VTT
PDG 2 Channel MD: 4*10UF(0603)+16*1UF(0402)
S360: channel B:2*10UF(0402)+ 2*1UF(0201)+2*4.3UF3T(P24)



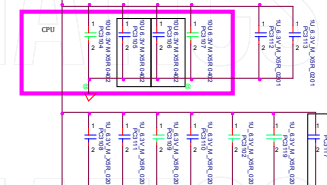
VPP
PDG 2 Channel MD: 5*10UF(0603)+16*1UF(0402)
S360: channel B: 2*10UF(0402)+8*1UF(0201)(P26)



VDDQ
PDG 2 Channel MD: 10*10UF(0603)+32*1UF(0402)
S360: channel B:5*10UF(0402)+ 4*1UF(0201)+3*4.3UF3T



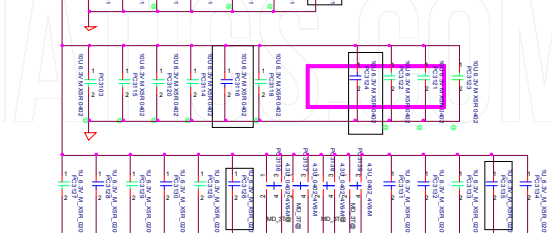
VDD2
+1.2V PDG: 2*47UF(0603)+ 8*10UF(0402)+8*1UF(0402)
S360: 4*22UF(0603 P93)+ 6*10UF+9*1UF



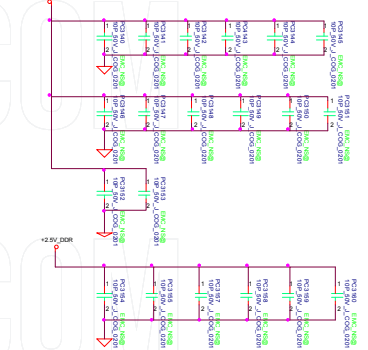
CHANGE VDD2 MLCC 0625

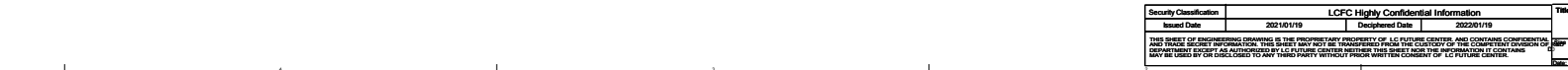
PDG: VDD2

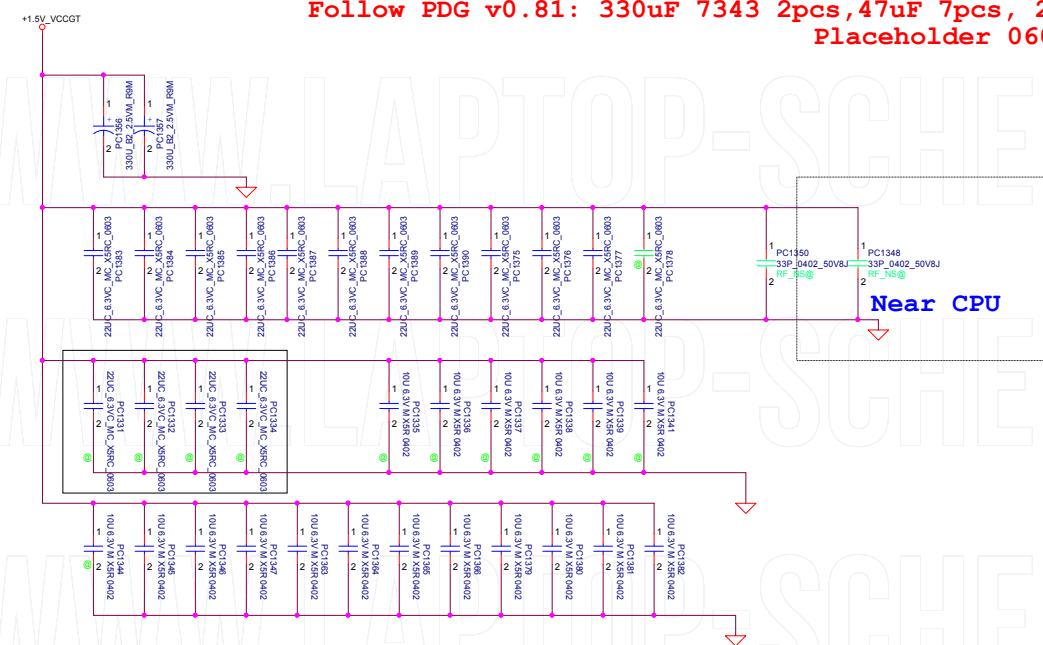
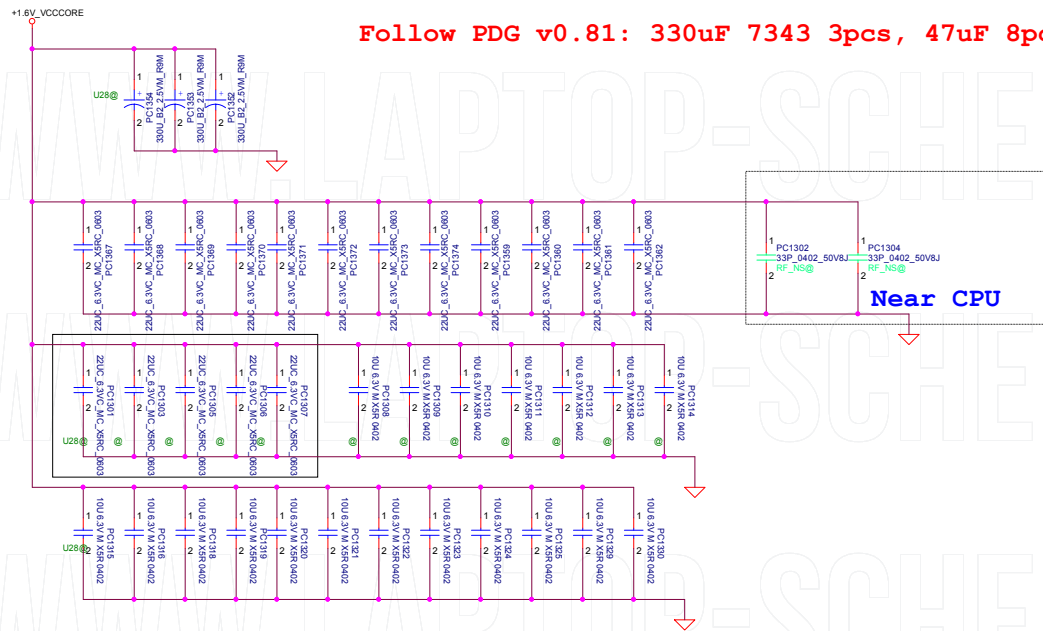
Value	Qty	Note
10u_0402	8	Place on the top edge of the board with a 0.5mm gap between the caps.
47u_0603	2	Placing these capacitors on the top edge of the board.
1u_0402	8	Place on the top edge of the board with a 0.5mm gap between the caps.



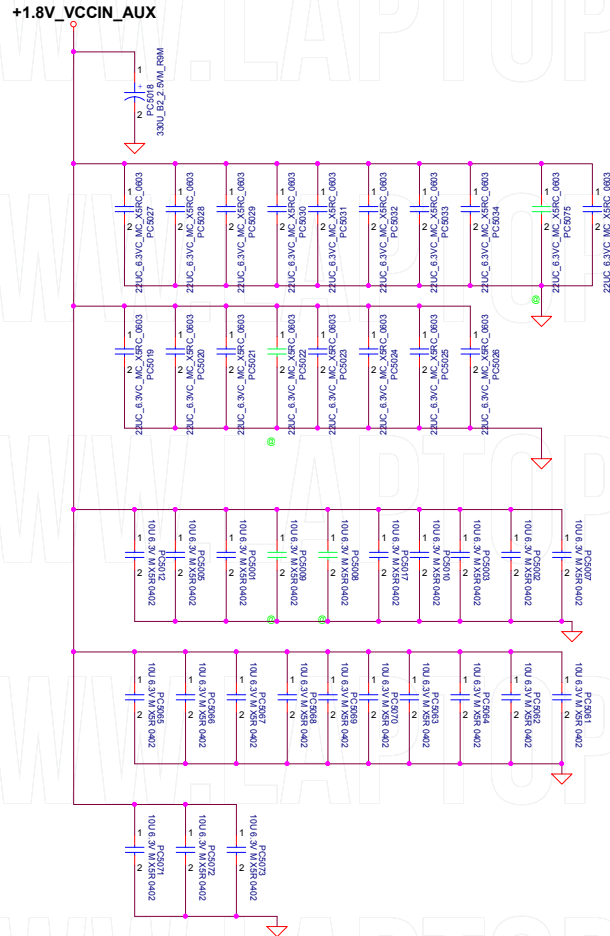
+1.2V







Follow PDG v0.81:330uF 7343 1pcs, CPU side 47uF*8, 10uF 10pcs



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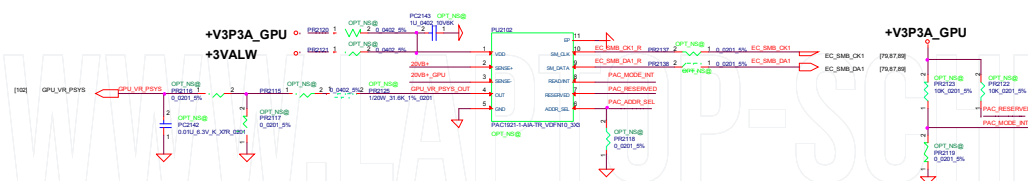
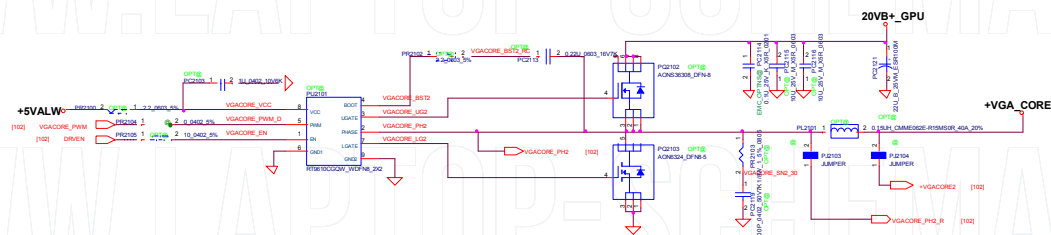
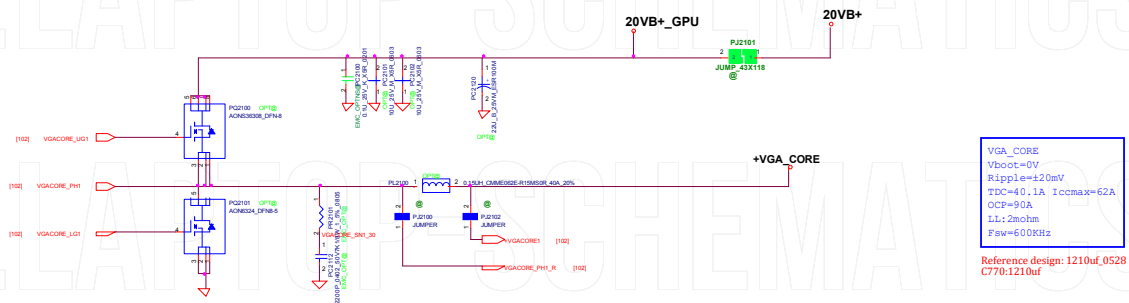
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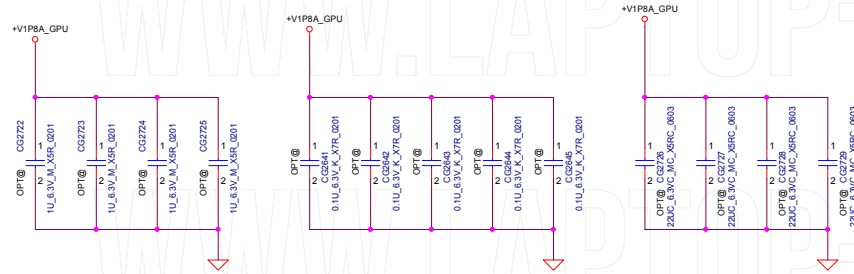
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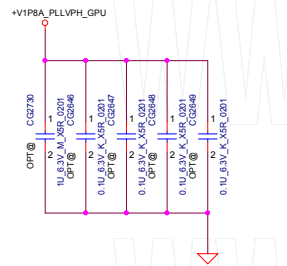
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+V1P8A_GPU RAIL



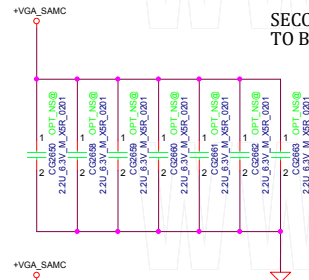
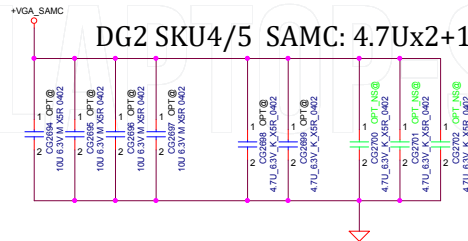
+V1P8A_PLLVPH RAIL



GPU DECOUPLING: VCCSAMC_GPU

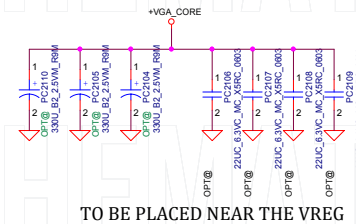
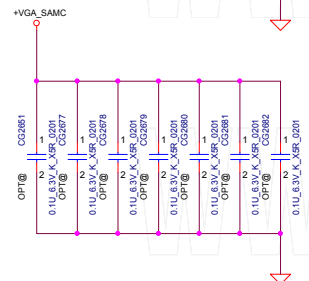
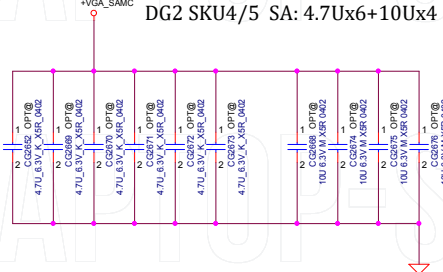
SECONDARY SIDE
TO BE PLACED CLOSE THE GPU

DG2 SKU4/5 SAMC: 4.7Ux2+10Ux4



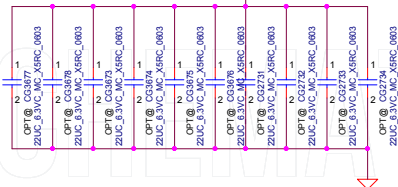
SECONDARY SIDE
TO BE PLACED CLOSE THE GPU

DG2 SKU4/5 SA: 4.7Ux6+10Ux4



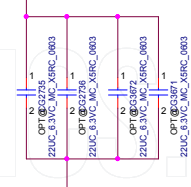
TO BE PLACED NEAR THE VREG

PRIMARY SIDE

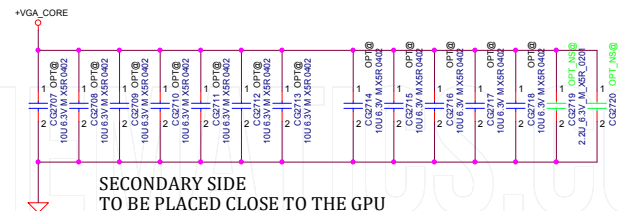


PLACEHOLDER (FOR SOCKET COMPENSATION)

+VGA_CORE



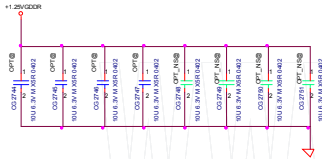
Follow AEP



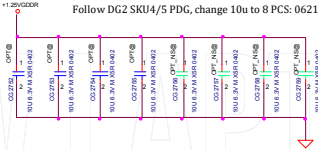
SECONDARY SIDE
TO BE PLACED CLOSE TO THE GPU

GPU GDDR DEVICE DECOUPLING

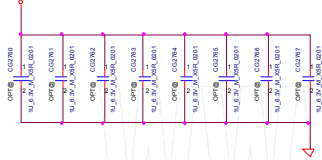
4 CAPS PER DRAM, 1 CAP PER EDGE/QUADRANT WITH VCCDDR & VCCDDRQ BGAS



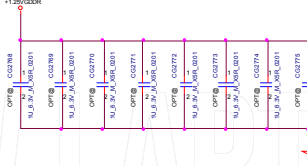
Follow DG2 SKU4/S PDG, change 10u to 8 PCS: 0621



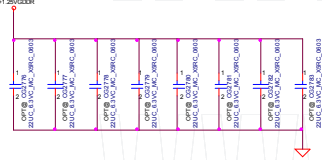
4 CAPS PER DRAM, 2 CAP PER EDGE/QUADRANT WITH VCCDDR BGAS



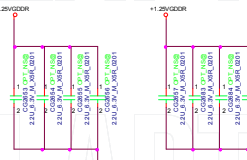
4 CAPS PER DRAM, 2 CAP PER EDGE/QUADRANT WITH VCCDDRQ BGAS



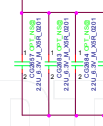
2 CAPS PER DRAM ON EACH SIDE OF POWER ENTRY



GPU DECOUPLING: VCCDDR_GPU VCCDDRQ_GPU

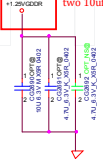
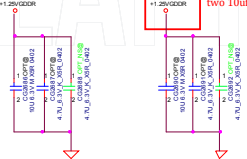


SECONDARY SIDE TO BE PLACED CLOSE TO GPU



Change 2.2u to 4.7u

two 10uF, two 4.7u, 0621



Change List

5					4					3					2					1				
Change List																								
D																								
C																								
B																								
A																								
5					4					3					2					1				

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Size B	Document Number				Rev 0.1
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Change List PWR